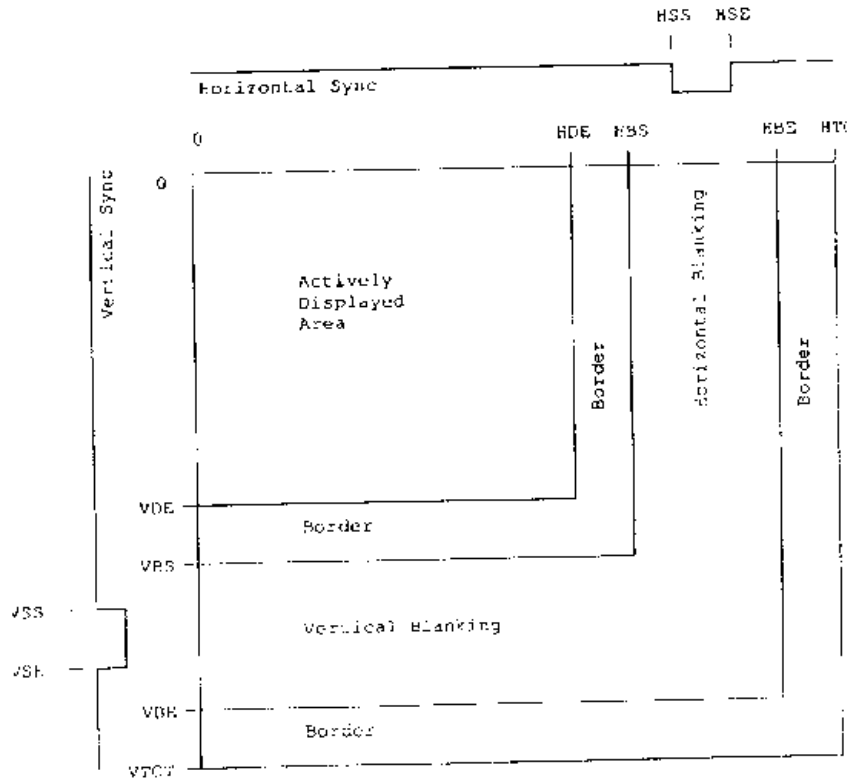
Contents

VGA CRT Controller (CRTC)

ET4000/W32 internal CRT Controller provides a 20-bit linear doubleword address, cursor control, and Vertical Sync
lorizontal Sync controls to external raster-scan CRT displays. Internally, the CRTC derives all reference timing in two
nsions: the horizontal display/blanking/sync and vertical display/blanking/sync. Each cycle in horizontal and vertical
olved around the ET4000/W32's CHARACTER and LINE reference logic. Each character is based on a multiple of
MCLK periods. Both CHARACTER and LINE reference logic can be asynchronously initialized via the SYNR input

diagram below displays the role that the CRTC registers play to effect the horizontal and vertical timings of the CRT.

re 2.1-1: CRTC Video Timing Control Registers



HDE: Horizontal Display End
HBS: Horizontal Blank Start
HBE: Horizontal Blank End
HSS: Horizontal Sync Start
HSE: Horizontal Sync End
HTOT: Horizontal Total

VDE: Vertical Display End
VBS: Vertical Blank Start
VBE: Vertical Blank End
VSS: Vertical Sync Start
VSE: Vertical Sync End
VTOT: Vertical Total

2.2 Secondary CRT Controller (CRTCB)/Sprite

This module of the ET4000/W32 may be programmed as a hardware cursor (Sprite) or as a secondary display window (CRTCB). The two features cannot, however, be used at the same time. A control bit is provided in the CRTCB/Sprite Control Register (Index: EF) to select between the CRTCB and Sprite functions.

The ET4000/W32 can be programmed to inform the host processor when the last scan line of the CRTC, or CRTCB/Sprite has been displayed on each frame using a system interrupt. See Section 5.3.32, CRTC Index Register 35, bit 6.

2.2.1 CRTCB Overview

The CRTCB is a secondary CRTC display window. Its X/Y position, X/Y size, starting address, width, and color depth can be programmed via the CRTCB registers (see Section 5.7). The main differences between CRTC and CRTCB are:

1. CRTCB is programmed relative to the CRTC's X/Y display window in terms of X/Y position and width in pixel (X) and line (Y) resolution. The size of the CRTCB display can be programmed from 1 pixel x 1 line, to the entire CRTC display size.

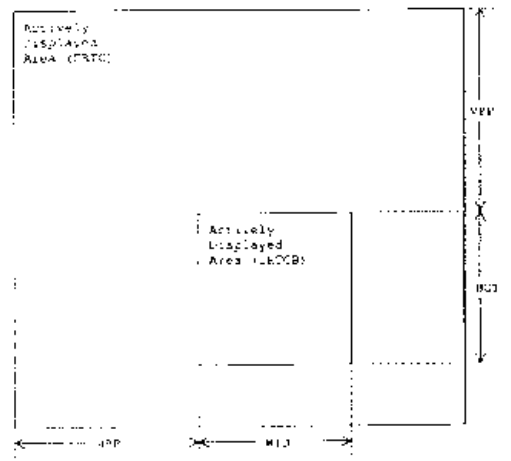
2. The color attributes displayed are not subject to internal "ATC" processing; i.e., the CRTCB display is packed pixel (linear graphics) format only.

3. The CRTCB display must be overlayed when the CRTC display is in timing state "1" (8 dots per character); i.e., CRTCB is always in 8 dots per character mode regardless of the CRTC's timing state.

2.2.2 Positioning the CRTCB Window

The CRTCB position on the screen is defined by the Pixel Position Registers. These registers indicate the point on the screen, relative to the actively displayed area of the CRTC, where the upper left-hand corner of the CRTCB window is displayed. The Width and Height Registers are used to control the pixel size of the CRTCB window. The following figure shows the use of these registers.

Figure 2.2.2-1: CRTCB Window Positioning



2.2.3 CRTCB Data Format

The data for the CRTCB window is stored in the display memory. The exact location of the beginning of the data in display memory is programmed into the Starting Address Registers, and the number of doublewords from one row of data to the next is programmed into the Row Offset Registers.

The Color Depth Register controls the formatting of the pixel data in memory.

	Byte 3								Byte 2								Byte 1								Byte 0							
bit w/in dword	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
bit w/in byte	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1 bpp																																
pixel number	24	25	26	27	28	29	30	31	16	17	18	19	20	21	22	23	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7
bit significance	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2 bpp																																
pixel number	12	12	13	13	14	14	15	15	8	8	9	9	10	10	11	11	4	4	5	5	6	6	7	7	0	0	1	1	2	2	3	3
bit significance	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
4 bpp																																
pixel number	6	6	6	6	7	7	7	7	4	4	4	4	5	5	5	5	2	2	2	2	3	3	3	3	0	0	0	0	1	1	1	1
bit significance	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0	3	2	1	0
8 bpp																																
pixel number	3	3	3	3	3	3	3	3	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
bit significance	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
16 bpp																																
pixel number	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
bit significance	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

2.2.4 Sprite Overview

The Sprite is a 64x64-pixel image. When active, it overlays the picture that is being displayed in CRTC. Each Sprite pixel is 2 bits, encoded to have the following effect on the display:

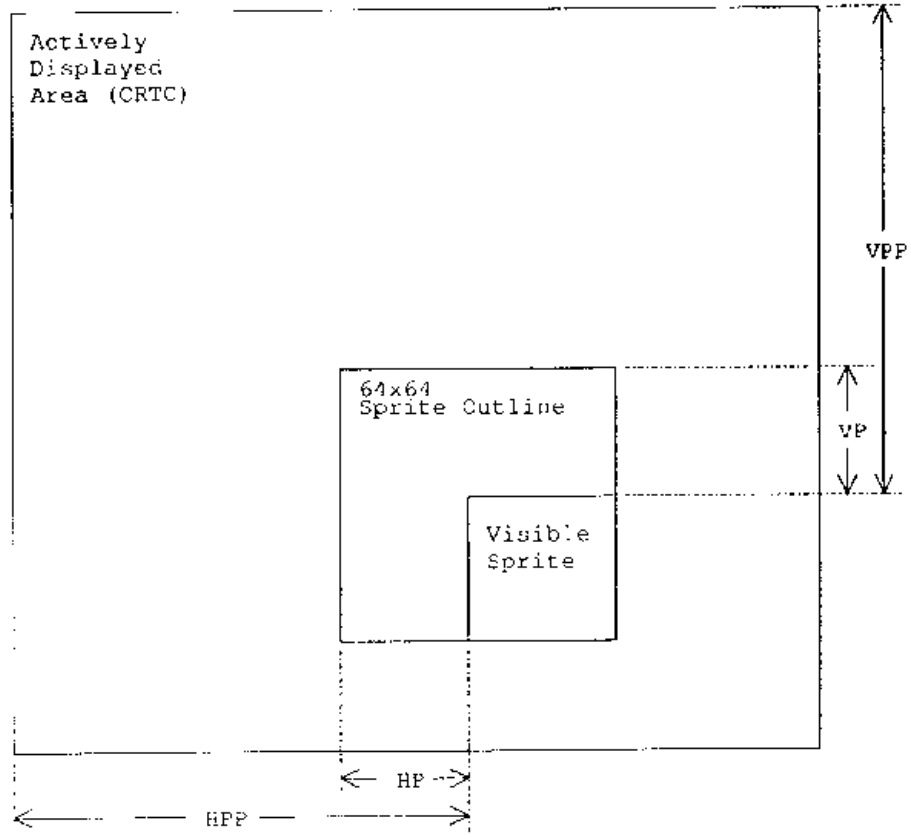
Bits<1:0>	Sprite Effect
0 0	Sprite Color 0 (defined as 00)
0 1	Sprite Color 1 (defined as FF)
1 0	Transparent (allow CRTC pixel through)
1 1	Reserved

2.2.5 Positioning the Sprite

The Sprite position on the screen is defined by two types of registers: Pixel Position, and Preset. The Pixel Position registers specify where the first displayed Sprite pixel (upper left-hand corner) appears on the screen, and the Preset registers specify the offset into the 64x64 Sprite buffer as well as the X/Y size of the visible portion of the Sprite.

The main use of the Sprite Preset registers is to allow for displaying sprites which are less than 64x64 pixels in size.

Figure 2.2.5-1: Sprite Positioning



HPP: Horizontal Pixel Position
HP: Horizontal Preset
VPP: Vertical Pixel Position
VP: Vertical Preset

2.6 Sprite Data Format

The data for the Sprite is stored in the display memory. The exact location of the beginning of the data in display memory is programmed into the Starting Address Registers. The data is stored in a contiguous 1024 byte area, arranged in the following linear "packed" format:

	Byte 3								Byte 2								Byte 1								Byte 0							
bit w/in dword	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
bit w/in byte	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
pixel number	15	15	14	14	13	13	12	12	11	11	10	10	9	9	8	8	7	7	6	6	5	5	4	4	3	3	2	2	1	1	0	0
bit significance	3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

A single row of the Sprite thus occupies 4 contiguous doublewords. The second row occupies the next 4 contiguous doublewords after the first row, and so on in an increasing fashion.

2.3 Memory Control Unit (MCU)

The Memory Control Unit provides programmable control of several aspects of the DRAM memory operation:

Memory control: RAS/CAS/MW timing/sequence control; the trp (RAS pre-charge), trcd (RAS to CAS delay), tcas (CAS pulse width), and tcp (CAS pre-charge), are programmable via CRTC Indexed Register 32.

Memory address: provides up to 4 megabyte addressing space via multiplexed AB<9:0> and AA<9:0> address interface.

Memory data: provides from 16-bit display memory data width to 32-bit data width via MD<31:0> data interface.

Memory refresh: programmable refresh frequency via CRTC Indexed Register 36.

2.4 System Priority Controller (SPC)

The SPC's main task is to maximize performance by orchestrating the ET4000/W32's internal resource requests including: the Display FIFOs, Graphics Data Controller, Multiport Cache Controller, Accelerator, Image Port, and RAM refresh. The available memory bandwidth for system performance is based on two major factors: the CRTC's demand (i.e., the display resolution and color), and the memory bandwidth (i.e., the memory bus width and access time). Use of the Graphics Accelerator and/or the Image Port can substantially increase performance by reducing the number of host accesses.

Other factors also can contribute to the overall performance. For example, the cache controller provides optimum performance for sequential access rather than random, and host write operations are generally faster than host read operations. The 32-bit Local Bus interface also results in faster data transfer, particularly in the plane graphics mode (a 32-bit CPU write equals up to a 128-bit data transfer). For further discussion of performance aspects, refer to Display Memory Design Considerations, Section 6.3.

2.5 Multiport Cache

The internal Multiport Cache™ an exclusive feature of the ET4000/W32, allows access of multiple masters to the display memory cache simultaneously. Multiport Cache provides the ET4000/W32 with the ability to parallel-process tasks. Even if the IMA port is updating an active second display window while the CPU and Accelerator processor are updating the primary active display, the ET4000/W32 will allow all three masters to read/write into the display memory, while operating concurrently.

2.6 Timing Sequencer (TS)

The Timing Sequencer module is responsible for providing basic timing control for both the CRTCs and ATC. Timings controlled by the TS registers include:

-Horizontal count resolution: 8 or 9 dots/character
-MCLK/2, MCLK/4, and DCLK/2 (dotclock)

2.7 Graphics Display Controller (GDC)

The GDC assists the CPU in manipulating pixel data that is in planar format in display memory. This includes rotate/mask/z-plane, with any of four boolean functions--- in response to a single CPU write. By putting basic bit map operations in high-speed hardware, the ET4000/W32 dramatically increases graphics processing throughput over software-driven solutions. The data manipulation capability implemented in the GDC is, however, applicable only for Plane systems and not for Linear Byte systems. This is because all the processing functions are designed to manipulate pixel data with one bit sourced from each plane. For example, the color compare function allows four bits across four planes (one pixel) to be compared to a pre-defined color, thereby allowing eight pixels to be color-compared simultaneously by processing 32 bits of video data (one byte from each plane).

2.8 Attribute Controller (ATC)

The internal Attribute Controller (ATC) provides flexible high-speed video shifting and attribute processing, and video load control every 8, 16, or 32 dot clocks, designed for both text and graphics video display applications. The ATC can process up to 16 bits of display data at the rate of 50MHz or 8-bit pixel data at a rate of 86MHz. In graphics modes, memory bits are reformatted into pixel color data in groups of 16, 8, 2, or 1 adjacent bits, translated through an internal 16-element color look-up table, and sent out serially to the video display. Through this pixel mapper, the ATC supports "PLANE" (for 16 colors), "BYTE" (256 colors) and "WORD" (65,536 colors) oriented pixel structures.

In text mode, eight bits of character code data and eight bits of attribute data are loaded; the character code is used as a lookup into a font table that is then loaded as the 16 bits of font data. The attribute is then applied to the font/cursor data, translated through the color lookup table, and sent out serially to produce 16 colors of text pixel data at speeds of up to 56MHz.

2.9 Image Port (IMA)

The Image Port is an 8-bit asynchronous input port capable of accepting CPU or image data directly into the display memory, and the ET4000/W32 will keep track of linear addresses being transferred as well as data transfer counts per line. The input data scan sequence can be interlaced, or non interlaced, and may be sent along with a bit mask so that only the differential motion data is transferred. Once in display memory, the IMA data may be displayed through either the primary display (CRTC), or the secondary display (CRTCB). The combination of the internal bandwidth of the W32 chip, along with the IMA port, make possible 640x480, 16.7 million color, full-motion (30 frame/second) digital video on desktop computer systems. The ET4000/W32 integrates Multimedia and Imaging capabilities beyond any SuperVGA class graphics controller.

The IMA port is a physical interface between an asynchronous processor such as an image processor for motion video, or simply a dedicated microprocessor high-speed direct connection, and the ET4000/W32 controller. The main mechanisms of this high-speed direct connection are:

1. Sustained asynchronous throughput rate up to 40 MB/sec.
2. The address generation is two-dimensional and sequential and is fully specified via IMA Registers E0-E6 prior to the data transfer.
3. The synchronization of address generation is by way of Frame/Line and odd/even interface signals.
4. The range of data transfer per line is specified by programming the image transfer length registers (IMA F3-F4).
5. A byte mask input can be used to specify only the changing motion video data to be transferred to the ET4000/W32's frame buffer. The masked data transferred can be used to reduce the bandwidth requirement.

next line by adding the image row offset, and return the IXRD, indicating that the IMA Port is ready for data transfers.

If the interlace bit (IMA Indexed Register F7, bit 1) is set to:

0, then image row offset value is added
1, then twice image row offset value is added

This process is repeated.

2.10 Memory Management Unit (MMU)

The ET4000/W32 Memory Management Unit (MMU) provides a mechanism to access the full 4MB range of display memory even though the display memory may occupy a much smaller region in the system's memory space. This is accomplished by providing a fixed-size "aperture" through which the display memory may be accessed. The aperture varies in size depending upon the system configuration; for typical VGA-compatible systems the aperture size is 8KB. See the Video Memory Map table in Section 7.3 to see how aperture size is related to system configuration. The aperture may be relocated to begin on any byte boundary in the 4MB display memory space.

2.10.1 Software Considerations

Each aperture has a Memory Base Pointer Register (MBP) which is 22 bits wide. The MBP Register specifies the starting address of the aperture in the linear display memory.

The MMU provides three independent apertures. The host implicitly selects which aperture to use by virtue of the address the host is accessing. As an example, consider the case of the MMU buffer space occupying the address region from B8000 through BDFFF (line six of the Video Memory Map table in section 7.3). All accesses in the range of B8000 through B9FFF will be directed through aperture number 0, BA000 through BBFFF use aperture number 1, and BC000 through BDFFF use aperture number 2. Figure 2.10.1-1 illustrates this address translation:

2.9.1 Image Port Interface Protocol

1. External Image Processor produces IXFS and IXLS pulses signaling initialization of linear address.

2. ET4000/W32 loads the image start address to the linear address generator.

   If the interlace bit (IMA Indexed Register F7, bit 1) is set to:

   0, then loads the image start address to the linear address generator.
   1, then (If IXOF = 1) loads image start address + image row offset to the linear address generator

      (If IXOF = 0) loads image start address to the linear address generator

3. After the trailing edge of IXLS and sensing IXRD ready acknowledgment, the image processor can begin to toggle the IXWQ* write request and place the 8-bit IM<7:0> and IDMK byte mask at each transfer. NOTE: IDMK, when equal to 0, can be used to "walk" the address generator's pointer without data being transferred.

4. The image processor continues to sample the IXRD ready (by clocking IXRD with the image processor's internal clock). If IXRD is asserted, the IXWQ* can be toggled, else IXWQ* is held at the high state.

5. If the number of doubleword count transfers has occurred, then IXRD will become inactive and wait for the IXLS input.

6. The image processor sends an IXLS line synchronization. If the IXLS input occurs before the doubleword count transfer is complete, the transfer counter is re-initialized to zero, and the remaining data will not be transferred.

7. Upon the leading edge of IXLS, the ET4000/W32 will advance the linear address pointer to the beginning edge of the

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Associated with each MMU aperture are two control bits:

- Linear Address Control (LAC), and
- Aperture Type (APT).

The LAC bit controls the organization of data in display memory for the given aperture. (See section 5.9 MMU Register Descriptions, MMU Control Register for a description of the LAC bits). The LAC bit allows the programmer to access memory in a linear fashion, independent of the current display mode.

The APT bit indicates that accesses through this aperture should be directed to the accelerator. Namely, if the APT bit is a "1", an access through this aperture will be passed to the accelerator; otherwise the access will go through the GDC to the display memory.

When the APT bit of an aperture is set to "0", the MBP for that aperture must be doubleword-aligned. This alignment restriction arises from the fact that the internal GDC cannot perform a multiple-cycle operation to memory, which would be required if an access crossed a doubleword boundary. The accelerator does not have any such restriction; so when the APT bit is set to "1", the MBP can point to any byte boundary.

Important Note: A read through an aperture with the APT bit set to "1" will return an undefined result. The chip does not allow data to be read from the accelerator.

The actual address translation that the MMU performs is quite simple. It adds bits <12:0> of the host address to the Memory Base Pointer for the selected aperture. If the Aperture Type bit is "1" and the host is supplying Mix Map data to the Graphics Accelerator, then the 13-bit host address is multiplied by 8 before being added to the Memory Base Pointer. This is done to compensate for the 8-to-1 ratio of "bytes processed" to "bits in the Mix Map". Figure 2.10.1-2 depicts the address translation process.

Figure 2.10.1-1 3 MMU Aperture Mapping

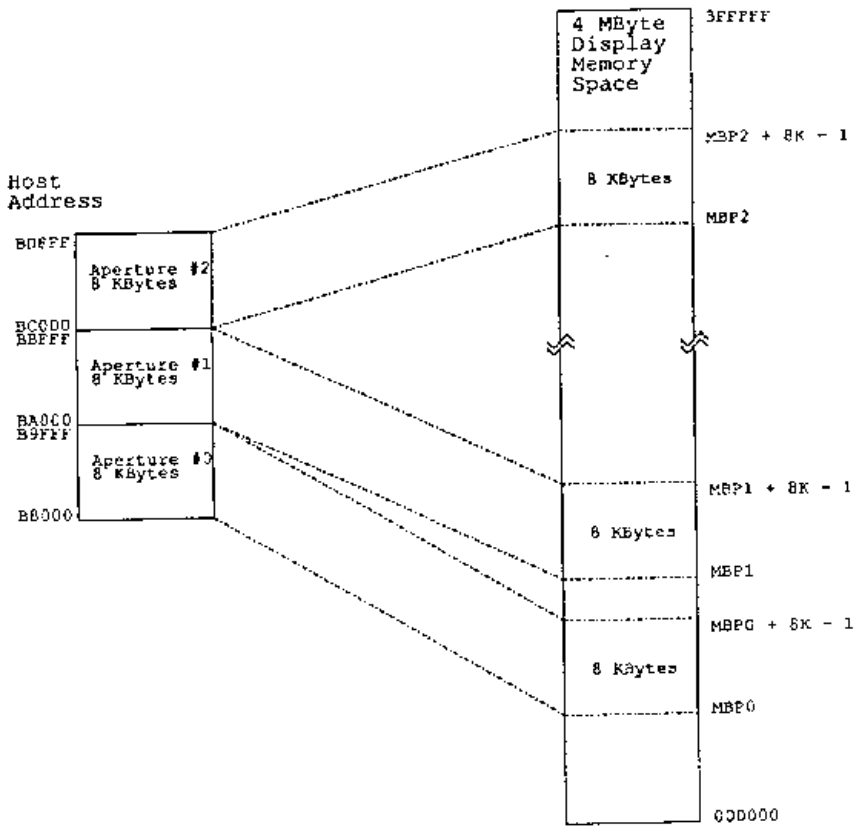
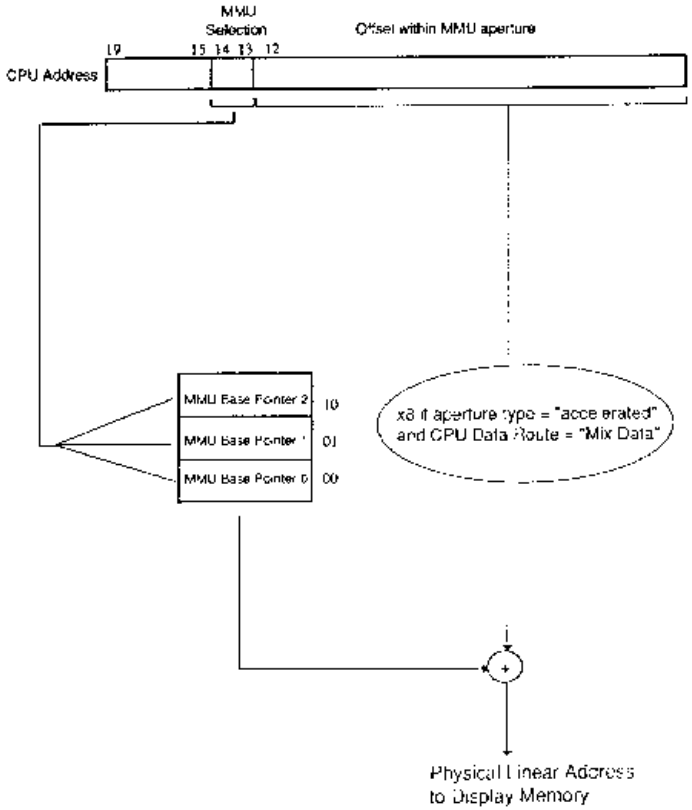


Figure 2.10.1-2: MMU Address Translation



2.10.2 Hardware Considerations

As mentioned earlier, the size of the aperture depends upon the system configuration. For example, if the image port is being used in a system linear-mapped configuration, only 20 bits of the host address can be wired to the chip (since the Image Port uses some pins normally used by the host address bus). In this configuration, bits 19 and 18 are used to select the aperture, while bits <17:0> are added to the Memory Base Pointer. The Video Memory Map in section 7.3 summarizes the effects of system configuration on the aperture size.

2.11 Graphics Accelerator (ACL)

The ET4000/W32 Graphics Accelerator is the most cost-efficient method to expedite functions used in common applications such as Microsoft Windows and other graphical user interface (GUI) software. Typically, personal computer architecture and processor performance limit the performance of operations such as BitBLT or Raster Operations. The ET4000/W32 allows the CPU to distribute these tasks to its Graphics Accelerator. The Accelerator is mapped to unused areas of the display memory address space, and reconfigures itself automatically when multiple adapters are present, or if the VGA switches from graphics into text mode.

The ET4000/W32 Graphics Accelerator provides a simple, yet powerful mechanism to accelerate the movement and processing of graphics data. The accelerator architecture adheres to the RISC philosophy of providing the basic building block for manipulation of graphics data at a high rate of performance, while allowing the software to manage the complexity of higher-level drawing algorithms. The accelerator has the capability to operate without CPU intervention on graphics data in the display memory, or it may take data from the CPU and mix it with data from the display memory.

Inside the accelerator are two primary functional blocks:

- An address sequencer, and
- A graphics data processor.

By using these two functions, much of the CPU-processing required to perform a Bit Block Transfer ("BitBLT") can be off-loaded from the host CPU to the Graphics Accelerator. The Address Sequencer maintains address pointers to locate data in display memory, and the Graphics Data Processor combines data from a Source Map, a Pattern Map, and a Destination Map, and writes it back to the Destination Map under the control of parameters programmed into the chip.

Maximum performance is achieved by:

- Minimizing the amount of information that must be passed across the host bus between the ET4000/W32 and the host processor.
- The CPU need not perform any combinatorial functions on the graphics data; all Raster Operations are performed by the Graphics Accelerator.
- For most rectangular BitBLT's, the CPU need not maintain address pointers.
- Accesses to the display memory are localized within the ET4000/W32, allowing the best possible utilization of display memory bandwidth.
- The CPU always has the option to maintain more control over a graphics operation, but still use the accelerator to assist in certain aspects of the operation. For example, the programmer may wish to have the CPU provide control of addressing the memory, but allow the accelerator to take care of applying the Raster Operation to the data.

2.11.1 Overview

The accelerator supports the notion of a "Pixel Map", which is defined by two things:

- A starting address in display memory, and
- A byte-offset from one scan line of the map to the next scan line.

The accelerator operates on four "Pixel Maps":

1. Source Map
2. Pattern Map
3. Destination Map
4. Mix Map

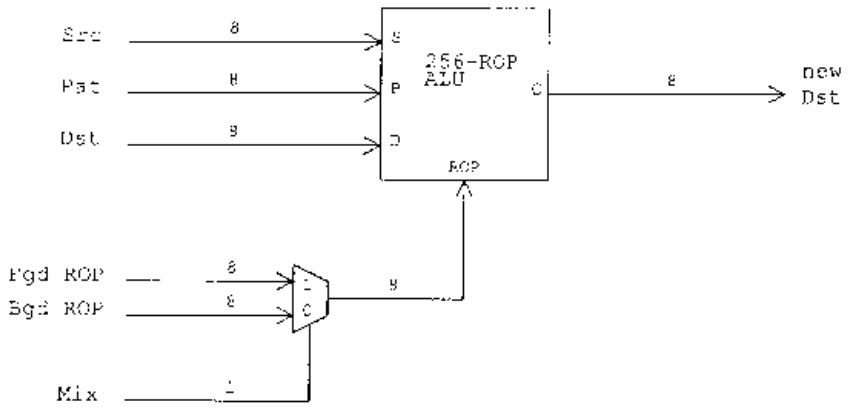
Data from these maps are combined according to the following rule:

D = FgdRop(S,P,D) if MixMap bit is 1
D = BgdRop(S,P,D) if MixMap bit is 0

The Foreground Raster Operation (FgdRop) and Background Raster Operation (BgdRop) are 8 bit values which cover any possible combinational mix of the three maps (Pattern, Source, and Destination). The encoding of these 256 ROP's is 100% compatible with the Microsoft Windows specification.

The Destination and Pattern maps must reside in the display memory. The Source map data may reside in display memory or be supplied by the CPU during an accelerated graphics operation. The Mix Map data may be supplied by the CPU, or it may be fixed to "1" (always use Foreground ROP). For a given graphics operation, the CPU can provide either Source data or Mix data (or neither), but not both. The Mix Map differs from the other three maps in that it is a "monochrome" map; that is, for each bit processed in the Mix Map, a byte is processed from the other three maps.

The figure below shows the path of one byte through the accelerator's Graphics Data Processor; in reality more than one byte is processed at a time.



ET4000/W32 Graphics Accelerator Data Path

11.2 Starting an Accelerator Operation

fter loading all the necessary accelerator control registers (e.g., X/Y Count Registers, Map Starting Addresses, Y Offsets, /Y Wrap values, Raster Operations, etc...), a graphics operation is initiated in one of two ways:

The host performs a write to the display memory, using the MMU Buffer Space. If the APT bit for the MMU aperture is "1", then an accelerator operation will begin. The address which is generated by the MMU translation is implicitly loaded into the Destination Address Register in the Accelerator Queue, and the accelerator operation is begun. Thus, the act of writing to the display memory using an MMU aperture which is in "accelerated mode" implicitly specifies that area of memory to be the Destination Map. ...OR...

The starting address of the Destination Map can be explicitly loaded into the Destination Address Register, and then a write to the Accelerator Operation State Register can be performed with both the "Resume" and "Restore" control bits set to "1".

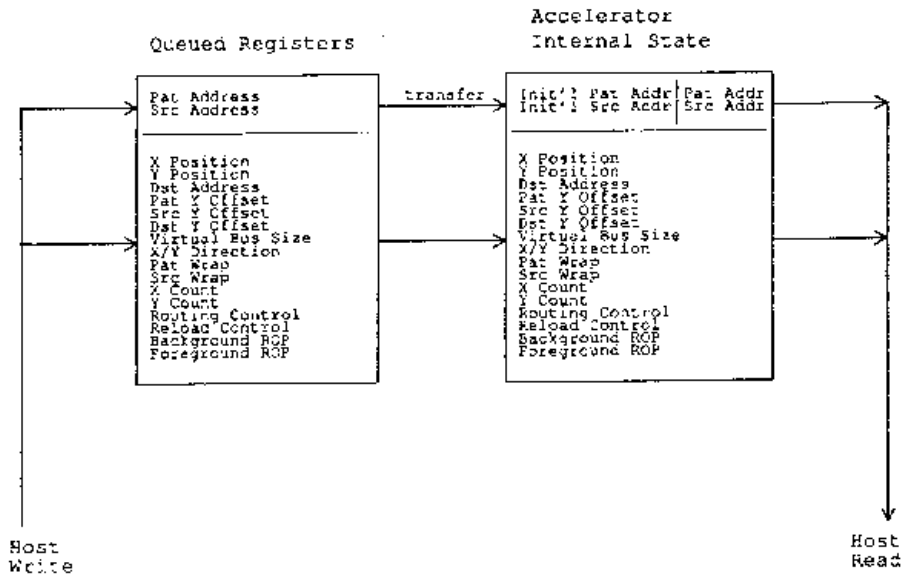
n accelerated graphics operation is defined as a two-dimensional "walk" through display memory. The X Count Register nd Y Count Register specify the limits of each dimension.

equential bytes are processed until the programmed limit of the X Count Register has been reached. At that time, each map's Offset is added to that map's starting address, and the X-walk is repeated. This sequence repeats until the programmed mit of the Y Count Register has been reached.

he accelerator always operates on pixel maps as if they are in linear format in display memory. The accelerator uses the MU only to translate the starting Destination Address. The accelerator does not use the MMU to perform any address anslations while it is performing a graphics operation. In other words, the MMU only operates on addresses from the host, nd never on internal addresses generated by the accelerator. This means that the programmer has complete freedom to alter ny MMU-related registers while the accelerator is in the middle of a graphics operation.

.11.3 The Accelerator's Queue

The ET4000/W32 has a one-level queue of registers for the Graphics Accelerator. In addition to the queue, there are registers nternal to the accelerator that it uses as a "working set" while it is performing a graphics operation. This configuration allows he host to be modifying the registers in the queue while the accelerator is running. The figure below shows the data path etween the host, queued registers, and accelerator registers. For most graphics operations, the queue starts out as being empty" and the host will load the registers in the queue to set-up the operation. Then the host will initiate the operation y one of the two methods outlined previously. At the time when the operation is initiated, the queue becomes "full" and ll of the values stored in the registers in the queue are transferred into the accelerator's internal state. After the transfer, he queue becomes "empty" again, waiting for the host to set-up the next operation.



ET4000/W32 Queued Registers and ACL Internal State

The queued registers retain their values after the transfer takes place, so the programmer need not load the entire queue for each graphics operation.

Since only the internal state of the accelerator is readable by the host, the host cannot simply read back a value that it has just written to a register in the queue. If the host wishes to read the contents of the queue, it must first cause a "transfer" to take place to move the data from the queue into the accelerator's internal state. This transfer is achieved by writing to the ACL Operation State Register with bit 0 (the "Restore" bit) set to "1". Naturally, the host must ensure that the accelerator is idle when the Restore is performed. There is a slight difference in the storage of the Source and Pattern Address Registers; the Restore operation shifts the data from the queue into the Initial Source, Pattern Registers, while the data in the Initial Source, Pattern Registers is moved into the internal Source, Pattern Address Registers of the accelerator. In other words, the Source and Pattern Address Registers are configured as a three-stage shift register, with the Restore operation triggering a shift by one. Conversely, all of the other registers are configured as a two-stage shift register.

2.11.4 Accelerator Operation

The accelerator maintains internal copies of the Source Address, Pattern Address, and Destination Address Registers which it increments as an accelerator operation progresses. The CPU may use the internal Source and Pattern Address Registers as the starting point of a subsequent accelerator operation by setting the appropriate bits in the ACL Reload Control Register (see Section 5.10.21). After an accelerator operation has completed, the internal Source Address Register (and/or Pattern Address Register) will point to the first byte of the next scan line to be processed. For example, if a BitBLT is initiated from (0,0) with a width of 4 (XCNT=3), a height of 2 (YCNT=1), and a Direction of X/Y Increasing (DIR=00), then the final Source Address will be the linear address that corresponds to the byte at an X/Y-position of (0,2).

The accelerator also maintains an internal copy of the X Position and Y Position as an accelerator operation progresses. These position registers serve as a "reference" pointer into each of the maps to indicate how far the operation has progressed. The X Position and Y Position Registers should be initialized to zero when the system is powered-up, and if they need to be loaded with non-zero values for a State-Save, they should subsequently be loaded with zero before resuming operation. In other words, the programmer should ensure that the X Position and Y Position Registers in the queue are zero before any graphics operation is begun; but it is not necessary to spend time loading the registers before every operation.

The internal address register for a map is only updated if that map is needed to perform the programmed Raster Operation. If the host is supplying Source data, the Internal Source Address Register (ISA) will not be altered. Basically, by using the Address-Route (ADRO) and Data-Route (DARO) control fields in the ACL Routing Control Register (see Section 5.10.20), the programmer can perform the following types of operations:

ADRO	DARO	Data Movement	Address Step	Notes
00	000	Screen-to-Screen	BLT	No host involvement, all maps in display mem
00	001	Host-to-Screen	BLT	Src data from host
00	010	Host-to-Screen	BLT	Mix data from host (e.g., Color Expansion)
01	000	Screen-to-Screen	host controls	e.g. draw circle, line, etc., pixel-by-pixel
01	001	Host-to-Screen	host controls	host provides Src data
01	010	Host-to-Screen	host controls	host provides Mix data
0x	100	Screen-to-Screen BLT	host provides	X Count (e.g., draw line segment)
0x	101	Screen-to-Screen BLT	host provides	Y Count (e.g., draw line segment)

NOTE: All functions feature 3-way ROP between Src,Pat,Dst, with ROP selected by the MixMap.Pattern is always assumed to be in the display memory. The MixMap data can be fixed to "1", or be provided by the host; it cannot originate from the display memory.

2.11.5 Passing Map Data to the Accelerator

2.11.5.1 Virtual Bus Size

To specify the passing of data from the host to the accelerator, the concept of "Virtual Bus Size" has been developed. The Virtual Bus Size is used to eliminate the effects of different physical system buses on the way data is transferred to the accelerator. The Virtual Bus Size allows the chip to be programmed and to function in the exact same manner whether it is connected to an 8-bit system bus or a 32-bit system bus, for example.

The Virtual Bus Size can be programmed to 1-byte, 2-bytes, or 4-bytes. Internally, the Host Interface of the ET4000/W32 "waits" for this many bytes, then releases the data to the accelerator. The Virtual Bus Size is only enforced when the CPU is passing Source or Mix Map data to an accelerated operation; all other writes to the chip operate normally. If the Virtual Bus Size is programmed to match the size of data transfer that is being done in the host assembly language, the accelerator will always give correct results no matter how many bus cycles are required to transfer the data, and no matter what address-order the bus cycles are in.

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Several important restrictions arise from this approach:

1. All CPU double-word writes to the accelerator must be double-word aligned.
2. All CPU word writes to the accelerator must be word aligned.
3. No restrictions on byte writes.

Once again, it is important to understand that these restrictions are only for writes of Source or Mix Map data to the accelerator; there are no restrictions on ordinary reads/writes to registers or to the display memory.

To handle word or double-word writes to an unaligned Destination map, the MMU Memory Base Pointer Register can be set to any byte boundary. This permits the ET4000/W32 to manage all unaligned data, while the CPU acts as if the map is aligned. This also maximizes performance by eliminating double or triple bus cycles on the host bus.

If the host is supplying Source or Mix data and the XCNT is not a multiple of the number of bytes specified by the Virtual Bus Size, then the "extra" bytes at the end of the line will be ignored.

Note that the Address Registers contain byte addresses, so if a BLT is moving in the "Decreasing-X" and "Decreasing-Y" direction, the initial Pattern Address, for example, should point to the last byte of the Pattern map. This is independent of the programmed Virtual Bus Size. The Destination Address, however, is dependent on Virtual Bus Size. If a write through an MMU aperture is initiating the operation, the write should address the last "Virtual-Bus-Sized" element of the Destination Map. For example, if VBS is 4-bytes, the initiating write should address the last doubleword of the Destination Map. The Accelerator internally takes care of pointing to the correct starting byte.

2.11.5.2 Synchronization

Another important issue when passing data from the host to the accelerator is synchronization. What we have here is two processors (the host and the accelerator) working in concert to perform a BitBLT. The transfer of data must be throttled so that the two processors remain in sync. This throttling can be done at one of two levels, the software level or the hardware level.

At the software level, the host can poll the Write-Status bit before each write to determine if there is room in the queue for another data write. Of course, this can add overhead to the inner loop for writing data to the accelerator, and is not generally recommended.

At the hardware level, the host bus WAIT (aka Ready) line can be used for synchronization. Programming the Sync Enable bit to "1" forces the ET4000/W32 to insert wait-states into a host data transfer when the queue is full. The primary concern when operating in this fashion is to limit the amount of time that the host bus is held waiting, since inordinately long wait times can crash some PC systems since the main memory cannot be refreshed. For this reason it is important to try to match the speed of the accelerator to that of the host processor. A general rule of thumb is to set the Virtual Bus Size to the largest value possible (usually 4 bytes) when passing Source Map data; and set to one byte when passing Mix Map data.

2.11.5.3 Data Alignment

When the host is supplying the Mix Map for a graphics operation, the processing order of bits in the Mix Map varies depending on the programmed X Direction:

- If the X Direction is increasing ("0"), the least significant bit of the Mix data is processed first. In other words the least-significant bit of the Mix Map is anchored to the left-most edge of the Destination Map.
- If the X Direction is decreasing ("1"), the most-significant bit of the Mix data is processed first. In other words the most-significant bit of the Mix Map is anchored to the right-most edge of the Destination Map.

11.6 Support for Common Graphics Operations

his section offers programming suggestions to perform some common graphics operations. This is by no means an haustive discussion; the programmer is encouraged to gain an understanding of the core functions that the Graphics celerator provides and decide how to best put them to use for specific operations.

11.6.1 Line Drawing

he Graphics Accelerator can draw vertical, horizontal, and diagonal (slope of +1 or -1) lines by appropriate programming f certain registers:

XCNT	YCNT	Y OFFSET	TYPE OF LINE
n-1	0	don't care	Horizontal
0	n-1	w-1	Vertical
0	n-1	(w-1) + 1	Diagonal

where: n = length of line (in bytes)
w = width of pixel map (in bytes)

ny line drawn using Bresenham's algorithm is made up of smaller line segments which are all horizontal, or all vertical, all diagonal. The only difference among these smaller line segments is the length of the segment. The accelerator allows e programmer to specify a destination starting address and the length (XCNT or YCNT) with a single bus write cycle to e chip. Thus, the inner loop of a line drawing routine need only contain a single write to the chip (plus whatever algorithmic ocessing must be done), thereby minimizing the number of bus transfers required to the chip. It is important to note that ese write cycles must be a size of one byte, so the upper 4 bits (bits<11:8>) of the Count register must be previously loaded ith the necessary value. This type of accelerator operation is achieved by programming the DARO field in the ACL Routing ontrol Register (see Section 5.10.20) to be 4 (to load the X Count Register), or 5 (to load the Y Count Register).

or simplicity, the table shown above is for 1 byte per pixel. It is a simple task to adapt the table to other pixel depths. Below the same table, generalized to allow different pixel depths:

XCNT	YCNT	Y OFFSET	TYPE OF LINE
n * b - 1	0	don't care	Horizontal
b-1	n - 1	(w x b)-1	Vertical
b-1	n - 1	(w x b)-1 + b	Diagonal

where: n = length of line (in pixels)
w = width of pixel map (in pixels)
b = bytes per pixel

11.6.2 Tiled and Fixed-Color Fills

oth the Source and Pattern Maps can be programmed to "wrap" or "tile" as the graphics operation progresses. The ogrammed starting address for the map indicates the corner of the tile which will be repeated through the operation.

he Source and Pattern Maps can be configured as fixed-color maps by programming the X/Y Wrap values to 4-by-1. If e Destination is 8 bit-per-pixel), the 8-bit fixed color must be written into all four bytes of the Source (Pattern) maps. This n be thought of as an X Wrap value of one byte. Similarly, an X Wrap of two bytes can be achieved by duplicating the o bytes to fill the four bytes of the map.

2.11.6.3 Color Expansion

The accelerator is capable of expanding a 1 bit-per-pixel (monochrome) pixel map into an 8 bit-per-pixel map. This is accomplished by setting the Foreground ROP to "Src", and the Background ROP to "Pat", and supplying the 1 bit-per-pixel map as the Mix Map. A "0" in the Mix Map will result in the fixed color in the Pattern map to be written to the Destination, and a "1" in the Mix Map will draw the Source color into the Destination. Of course, it is also possible to make the Foreground ROP a function of the Source and Destination, and the Background ROP a function of the Pattern and Destination if this is required.

2.11.6.4 Clipping

For the most part, rectangular clipping must be done by the software; however, clipping with a data mask can be accomplished by using the Mix Map and programming the Background ROP to "Dest" and the Foreground ROP as desired. This allows each bit in the Mix Map to control whether the corresponding byte is processed or left alone.

2.11.7 Accelerator Interrupts

The ET4000/W32 is capable of generating a system interrupt on three possible conditions:

1. Write Interrupt - This interrupt is generated while the queue is in the state of being "not-full". This status indicates that the queue is ready for another write to it. This is a state-triggered interrupt; i.e., the interrupt line is asserted while the queue is in the state of being "not-full". The interrupt is cleared by disabling it (writing a "0" to bit 0 of the ACL Interrupt Mask Register).

2. Read Interrupt - This interrupt is generated when the queue is empty and the accelerator goes from busy to idle, indicating that the accelerator is no longer performing a graphics operation, and will not start to perform another operation without a command from the host. The terminology of "read interrupt" conveys the fact that the host is ensured of reading correct results from the display memory and from any of the accelerator registers that are modified during the course of an accelerated graphics operation. This is an event-triggered interrupt; i.e., the interrupt line asserts when the accelerator goes from busy to idle, and stays asserted until the interrupt is cleared (by a write of "1" to the corresponding bit in the ACL Interrupt Status Register).

3. Write Fault Interrupt - This interrupt is generated when the host writes to the queue when it is full and the Sync Enable bit is "0". Under these conditions, the write is ignored. This is an event-triggered interrupt; i.e., the interrupt line asserts when the host write occurs, and stays asserted until the interrupt is cleared (by a write of "1" to the corresponding bit in the ACL Interrupt Status Register).

2.11.8 Accelerator State Save/Restore

The ET4000/W32 provides a mechanism for suspending an active graphics operation, saving the state of the operation, restoring the state of an operation, and resuming the operation. This type of feature is often required by multi-tasking operating systems to allow several tasks to share the display hardware. Generally, the host will take an interrupt when a task-switch is required; the pseudo-code below outlines the steps required to save and restore the state of the Graphics Accelerator:

2.11.8.1 State-Save Interrupt Handler

```
Write "1" to bit 0 (SO) of ACL Suspend/Terminate Register.  /* suspends operation */
while (STAT.RDST==1)  /* wait for accel op to complete */
;
Write "0" to bit 0 (SO) of ACL Suspend/Terminate Register.
/* By now, accelerator is not doing anything */
Read all accelerator registers from chip (including STAT) and save into local array, called SAVE1.
Write "1" to bit 0 (RSO) of ACL Operation State Register.    /* "shifts" state from queue */
Read Source Address and Pattern Address Registers from chip and save into variables called ISA and IPA.
Write "1" to bit 0 (RSO) of ACL Operation State Register.    /* "shifts" state from queue */
Read all accelerator registers from chip and save into local array, called SAVE2.
Write "1" to bit 4 (TO) of ACL Suspend/Terminate Register.  /* terminates operation and resets accelerator */
while (STAT.RDST==1)  /* wait for Read-status OK */
;
Write "0" to bit 4 (TO) of ACL Suspend/Terminate Register.
Done with State Save.
```

2.11.8.2 State-Restore Interrupt Handler

```
Load the array SAVE1 back into chip (including STAT).
Write "1" to bit 0 (RSO) of ACL Operation State Register.    /* "shifts" state from queue */
Load ISA and IPA into Source and Pattern Address Registers.
Write "1" to bit 0 (RSO) of ACL Operation State Register.    /* "shifts" state from queue */
Load the array SAVE2 back into chip.
Write (SAVE1.STAT & 8) to ACL Operation State Register.  /* resume screen-to-screen op if necessary */
Done with State Restore.
```

3. ET4000/W32 Pin Descriptions

The ET4000/W32 provides a flexible interface to different types of CPU buses as well as options such as the image port, high color DAC, and hardware sprite. It is compatible with the following CPU buses:

- ISA 8/16 bits
- Micro Channel 8/16 bits
- Local Bus 386/486 SX/DX 16/32 bits
- VESA LBUS

A specific host bus type is selected by pulling the UCPC and AEN* input pins to appropriate levels at reset. A Power On Reset Initialize (PORI) scheme is used to determine different configurations for each bus type to ensure full hardware compatibility.

3.1 Power On Reset Initialize (PORI)

During the high to low transition of the REST signal, DB<15:0> is latched internally. These latched data bits are used to determine the host interface configuration. DB<15:0> are normally pulled high internally; these signals can be pulled down via a series resistor to ground, or driven low with a tri-state buffer during reset.

Description of terms

I	= Input
O	= Output
IO	= Bidirectional
PWR	= Power input pin
TTL	= Pin has standard TTL input and output thresholds
CMOS	= Pin has standard CMOS input and output thresholds
S	= Schmitt Trigger on input
TS	= Tri-state
OC	= Open-collector (these are actually tri-state outputs, driven low, float high)
PU	= Internal passive pull-up
PD	= Internal passive pull-down
B2	= Output buffer can source/sink 2mA
B4	= Output buffer can source/sink 4mA
B8	= Output buffer can source/sink 8mA
High	= Voltage level between 2.0V and VDD (also abbreviated "H")
Low	= Voltage level between VSS and 0.7V (also abbreviated "L")
*	= Active Low

Table 5.0-2 ET4000/W32 Mapped Registers, R/W Operation, Size

See Section 7.3 for the memory base address for the MMU and ACL registers. The offset in the table below is added to the base address to calculate the actual address of the register.

Register	R/W Operation*	Memory Offset	Bits
Memory Management Unit (MMU)			
MMU Base Pointer 0	RW	00	<21:0>
MMU Base Pointer 1	RW	04	<21:0>
MMU Base Pointer 2	RW	08	<21:0>
MMU Control Register	RW	13	<7:0>
Graphics Accelerator (ACL)			
Suspend/Terminate	RW	30	<7:0>
Operation State	WO	31	<7:0>
Sync Enable	RW	32	<7:0>
Interrupt Mask	RW	34	<7:0>
Interrupt Status	RW	35	<7:0>
Accelerator Status	RW	36	<7:0>
Pattern Address	RW	80	<21:0>
Source Address	RW	84	<21:0>
Pattern Y Offset	RW	88	<11:0>
Source Y Offset	RW	8A	<11:0>
Destination Y Offset	RW	8C	<11:0>
Virtual Bus Size	RW	8E	<7:0>
X/Y Direction	RW	8F	<7:0>
Pattern Wrap	RW	90	<7:0>
Source Wrap	RW	92	<7:0>
X Position	RW	94	<11:0>
Y Position	RW	96	<11:0>
X Count	RW	98	<11:0>
Y Count	RW	9A	<11:0>
Routing Control	RW	9C	<7:0>
Reload Control	RW	9D	<7:0>
Background Raster Operation	RW	9E	<7:0>
Foreground Raster Operation	RW	9F	<7:0>
Destination Address	RW	A0	<21:0>

* See Section 2.11.3 on reading and writing accelerator registers

5.1 General Registers

The ET4000/W32 has five General Registers, each with its own port address allowing direct programming access, and requiring no pairing of index and data registers. The Input Status #1 and Feature Control registers have separate addresses for monochrome and color modes.

5.1.1 Miscellaneous Output Register

I/O address = 3CC read; 3C2 write

Bit	Description	Access
7	Vertical Retrace Polarity.	RW
6	Horizontal Retrace Polarity.	RW
5	Page Select for Odd/Even.	RW
4	Reserved.	
3	Clock Select 1.	RW
2	Clock Select 0	RW
1	Enable RAM.	RW
0	I/O Address Select.	RW

Hardware resets return all bits to zero.

Bit **Description**

Bit 7 When set to 1, selects negative vertical retrace.

When set to 0, selects positive vertical retrace. The relationship between vertical screen size and polarities is as follows:

Vsync polarity	Hsync polarity	Vertical size
+	+	768 lines
+	-	400 lines
-	+	350 lines
-	-	480 lines

Bit 6 When set to 1, selects negative horizontal retrace polarity.

When set to 0, selects positive horizontal retrace polarity.

Bit 5 Selects between two 64K pages of memory when in the Odd/Even display modes (0,1,2,3,7).

When set to 1, it is the default for operation of the HiRes text mode.

When set to 0, selects the high page of memory.

Bits 3:2 Used to select the clock rate according to the following table:

Bits
3 2
0 0- Selects MCLK clock 1
0 1- Selects MCLK clock 2
1 0- Selects MCLK clock 3
1 1- selects MCLK clock 4

See Section 5.3.28, CRTC Indexed Register 34 for more information regarding clock selects.

Bits<3:2> of the MISCOUT register (CS<1:0>) can be translated to provide compatibility between the EGA mode and the EGA monitor when the external clock select circuit is connected as follows:

CS1	CS0	Clock Frequency
1	1	—
1	0	32.514MHz
0	1	28.322MHz
0	0	25.175MHz

The clock select bits CS<1:0> can be translated by the ET4000/W32 according to the following conditions:

NOTES: 1.EMCK = CRTC Index 34 bit 0 and ENXL = CRTC Index bit 5.
2.If CS<1:0> are used to select the external switch setting, care must be taken to ensure proper selection of the switch setting after the translation of CS<1:0>.

In VGA mode:

a. If EMCK bit is set to 0: CS<1:0> are equal to the programmed value.
b. If EMCK bit is set to 1: CS<1> is equal to the programmed value, and CS<0> is equal to inversion of programmed value.

In EGA mode:

a. if ENXL = 0 then:

programmed CS<1:0>; output CS<1:0>

1 1	0 0
1 0	1 1
0 1	1 0
0 0	0 1

b. if ENXL = 1 then:

1. If EMCK bit is set to 0: CS<1:0> are equal to the programmed value.
2. If EMCK bit is set to 1: CS<1> is equal to the programmed value, and CS<0> is equal to inversion of programmed value.

In 6845 modes: CS<1:0> are equal to the programmed value.

Bit 1 — When set to 1, enables access to display memory.

When set to 0, disables display memory access from the host.

Bit 0 — When set to 1, sets CRTC addresses to 3DX and Input Status Register 1's address to 3DA for Color/Graphics Monitor Adapter emulation.

When set to 0, sets CRTC addresses to 3BX and Input Status Register 1's address to 3BA for monochrome emulation.

5.1.2 Input Status Register Zero

I/O address = 3C2

Bit	Description	Access
7	CRT Interrupt.	RO
6	Feature code 1.	RO
5	Feature code 0.	RO
4	Switch Sense.	RO
3	Reserved.	
2	Reserved.	
1	Reserved.	
0	Reserved.	

NOTE: the "KEY" must be set in order to read bits 5 and 6.

To set the KEY:
- Write 03 to Hercules Compatibility Register (3BF);
- Write A0 to Mode Control Register (3#8);

```
mov     dx,3BFh
mov     al,3
out     dx,al
mov     dx,3D8h;3B8h in mono mode
mov     al,0A0h
out     dx,al
```

To turn OFF the KEY:

- Set 3D8 (or 3B8) to a value not equal to A0

Additionally:

- Set 3D8 = 29
  set 3BF = 1

Bit	Description
Bit 7	A value of 1 indicates a pending vertical retrace interrupt. A value of 0 means that the vertical retrace interrupt has been cleared.
Bit 6:5	Inputs can be used to determine the type of monitor connected to the system. Input status is from external feature input. NOTE: The external feature input bits 6 & 5 are DB<1:0> bus status at the last REST low-to-high transition. If the DB<1:0> are not "pull-down" by a 1K resistor, then a "11" status will be the default value.
Bit 4	Input can be used to determine the default video mode upon power-up, or the type of monitor connected to the system. The Clock Select field (bits 2,3 in the Miscellaneous Output Register) setting determines the switch to read.

5.1.3 Input Status Register One
I/O address = 3BA (mono)/3DA (color)

Bit	Description	Access
7	Vertical retrace complement.	RO
6	Reserved (=0).	
5:4	Video display feedback test.	RO
3	Vertical retrace.	RO
2:1	Reserved (=0).	
0	Display enable complement.	RO

Bit **Description**

Bit 7 A value of 1 indicates that video data is currently being displayed.

A value of 0 indicates the vertical blanking or vertical border time. (See Figure 2.1-1)

Bits 5:4 Used for diagnostic purposes. They are selectively connected to two of the eight color outputs of the Attribute Controller. The Color Plane Enable (ATC Indexed Register 12) register controls the multiplexer for the video wiring. Available combinations are:

Color Plane Register Bits		Input Status Register One Bits	
5	4	5	4
0	0	P2	AP0
0	1	P5	AP4
1	0	P3	AP1
1	1	P7	AP6

Bit 3 A value of 0 indicates that video data is currently being displayed.

A value of 1 indicates a vertical retrace interval during the vertical sync pulse.

Bit 0 A value of 1 indicates a vertical or horizontal retrace interval and is the real-time status of the inverted display enable signal.

5.1.4 Feature Control Register
I/O address = 3CA read; 3BA/3DA write

Bit	Description	Access
7	Enable NMI generation.	RW
6	Reserved.	
5:2	Monitor ID.	RO
1	Feat (1)	RW
0	Feat (0).	RW

NOTE: The "KEY" must be set in order to read bits 5:2, and 7. See Section 5.1.2, Input Status Register Zero for definition of "KEY".

Bit **Description**

Bit 7 When set to 1, enables a non-maskable interrupt (NMI). This bit can only be set when in 6845 compatibility mode (CRTC Indexed Register 34, bit 7=1).

Normally, the XROM* output pin is defined as external translation ROM enable. When bit 7 of the Feature Control Register is set to 1, the XROM* pin will be defined as the NMI output pin (See Section 6.9.4). This bit can only be set if the 6845 emulation mode is active.

Bits 5:2 Used to read back the MONID<5:2> pins (MONID<3:2> for Local Bus) for monitor identification. See also Section 5.1.2, Input Status Register Zero, bit 4 for monitor ID.

Bits 1:0 General purpose read/write bits. In previous designs these bits were output to the Feature Connector.

5.1.5 Video Subsystem Enable Register

I/O address = 3C3/46E8

The Video Subsystem Enable Register is accessible via one of two locations (03C3 or 046E8), selected by bit 3 of CRTC Indexed Register 34. If the Video Subsystem Enable Register is at 03C3, then bit 0 is the "Enable Video Subsystem" bit. The power-up default has this register at 03C3.

When the video subsystem is disabled, the chip does not respond to any host read/writes, except to the Video Subsystem Enable Register.

Bit	Description	Access
7:4	Reserved (=0).	
3	Enable video subsystem (address 46E8).	RW
2:1	Reserved.	
0	Enable video subsystem (address 03C3).	RW

Bit	Description
Bit 3	When set to 1, enables the video subsystem when the port address is configured for 46E8.
Bit 0	When set to 1, enables the video subsystem when the port address is configured for address 3C3.

5.2 6845 Compatibility

The ET4000/W32 features register-level compatibility with the 6845 chip. The input/output control ports used in setting up the basic display formats are as follows:

Port	I/O Port Address
6845 CRT control register	03#4
6845 CRT data register	03#5
Display mode control	03#8
Display color control	03D9
Display status control	03#A

5.2.1 Display Mode Control Register

I/O address = 3D8 (color)

Bit	Description	Access
7	Reserved.	
6	Bit 1 of the Hercules Compatibility Register (3BF).	RO
5	Enable blink (text mode only).	RW
4	640x200 mode.	RW
3	Enable screen display.	RW
2	B&W mode.	RW
1	Enable graphics mode.	RW
0	80x25 text mode.	RW

Bit	Description
Bit 6	Bit 1 of the Hercules Compatibility Register; a read-only bit.
Bit 5	When set to 1, changes the character background intensity to the blinking attribute function in A/N modes.
Bit 4	When set to 1, selects the 640x200 black and white graphics mode.
Bit 3	When set to 1, enables the video signal during mode changes.
Bit 2	When set to 1, selects the black and white mode.
	When set to 0, selects color mode.
Bit 1	When set to 1, selects the 320x200 APA mode.
	When set to 0, selects the A/N mode.
Bit 0	When set to 1, selects the 80x25 A/N mode.
	When set to 0, selects 40x25 A/N mode.

5.2.2 Display Mode Control Register

I/O address = 3B8 (monochrome)

Bit	Description	Access
7	Page select.	RW
6	Bit 1 of the Hercules Compatibility Register (3BF).	RO
5	Enable blink.	RW
4	Reserved.	
3	Enable screen display.	RW
2	Reserved.	
1	Monochrome graphics mode.	RW
0	80x25 text mode.	RW

Bit	Description
Bit 7	When set to 1, selects the top 32KB page starting at B8000 (for Hercules compatibility). When set to 0, selects the low 32KB page (starting at B0000). NOTE: This bit can be set only when bit 1 of the Hercules Compatibility Register (3BF) is set to 1.
Bit 6	Bit 1 of the Hercules Compatibility Register, is a read-only bit.
Bit 5	When set to 1, changes the character background intensity to the blinking attribute function in A/N modes.
Bit 3	When set to 1, enables the video signal during mode changes.
Bit 1	When set to 1, selects the monochrome graphics mode.
Bit 0	When set to 1, selects the 80x25 A/N mode. When set to 0, selects 40x24 A/N mode.

5.2.3 Color Select Register

I/O address = 3D9

Bit	Description	Access
7	Reserved.	
6	Reserved.	
5	320x200 color set select.	WO
4	Select intensified foreground colors in 320x200 APA mode.	WO
3	Intensified border color in A/N mode. Intensified bkgd color in 320x200 APA mode. Intensified fgd color in 640x200 APA mode.	WO
2	Red border color in A/N mode. Red bkgd color in 320x200 APA mode. Red fgd color in 640x200 APA mode.	WO
1	Green border color in A/N mode. Green bkgd color in 320x200 APA mode. Green fgd color in 640x200 APA mode.	WO
0	Blue border color in A/N mode. Blue bkgd color in 320x200 APA mode. Blue fgd color in 640x200 APA mode.	WO

This 6-bit output register determines the border color, background color, and color intensity.

Bit	Description
Bit 5	Used only in 320x200 graphics mode, is used to select an active set of colors for the screen display. When bit 5 is set to 1 the colors are as follows:

C1	C0	Colors
0	0	Background (defined by bits 0-3 at 3D9).
0	1	Cyan
1	0	Magenta.
1	1	White.

When bit 5 is set to 0 the colors are as follows:

C1	C0	Colors
0	0	Background (defined by bits 0-3 at 3D9).
0	1	Green.
1	0	Red.
1	1	Brown.

C1 and C0 are the high and low order bits, respectively, of the 2-bit pixel.

Bit 4	When set to 1, selects intensified foreground colors for 320x200 graphics mode.
Bits 3:0	Are used to select the background color in the 320x200 graphics mode, the foreground color in the 640x200 graphics mode, and the border color in the 40x24 alphanumeric mode.

5.2.4 AT&T Mode Control Register

I/O address = 3DE

Bit	Description	Access
7	Reserved.	
6	Underline color attribute enable.	WO
5	Reserved.	
4	Reserved.	
3	Alternate page select.	WO
2	Alternate font select.	WO
1	Reserved.	
0	Double scan line mode.	WO

This is an 8-bit write-only register used to produce 640x400 AT&T-compatible resolution. To enable this register, bit 7 of the 6845 Compatibility Control Register (CRTC Index 34) must be enabled. (Bit 6 is enabled just by bit 6 of CRTC 34; bit 0 requires both bits 6 and 7 of CRTC 34 to be set.) This register must be set while in color mode (Misc. Output Register bit 0 = 1).

Bit	Description
Bit 6	When set to 1 and the attribute byte (ATT) = 01, the normal blue foreground color attribute will be disabled and the white underline attribute of that character will be enabled.
Bit 3	Alternate page select, is used to select either of two 16KB pages in memory to be displayed. (NOTE: bit 0 must = 0 to get 2nd page.)
Bit 2	Alternate font select, is used to select one of two character fonts stored in font blocks 0 and 1 to be displayed. The font stored in font block 0 is the default font.
Bit 0	When set to 1, is a double-scan bit that simulates AT&T 400-line graphics. When set to 0, simulates IBM 200-line graphics.

5.2.5 Hercules Compatibility Register

I/O address = 3BF

Bit	Description	Access
7:2	Reserved.	
1	Enable second page.	WO
0	Reserved.	

Bit	Description
Bit 1	When set to 1, enables the second page of display memory, starting at B8000, providing 64KB of display memory. This bit can be read from bit 6 of the Display Mode Control Register (3#8).

The following table lists the 6845 CRT controller internal data registers, their functions, and the hexadecimal values used for the illustrated modes.

Table 5.2-1 6845 Color CRT Controller Registers, Functions, and Parameters

		TEXT		GRAPHICS
		80	40	320x200
	Register	x	x	4-color
Register	Number	25	25	2-color
Horizontal Total	R0	71h	38h	38h
Horizontal Displayed	R1	50h	28h	28h
Hsync Position	R2	5Ah	2Dh	2Dh
Hsync Width	R3	0Ah	0Ah	0Ah
Vertical Total	R4	1Fh	1Fh	7Fh
Vertical Adjust	R5	06h	06h	06h
Vertical Displayed	R6	19h	19h	64h
Vsync Position	R7	1Ch	1Ch	70h
Interlace Mode	R8	02h	02h	02h
Max. Scan Line Addr.	R9	07h	07h	01h
Cursor Start	R10	06h	06h	06h
Cursor End	R11	07h	07h	07h
Start Address (H)	R12	00h	00h	00h
Start Address (L)	R13	00h	00h	00h
Cursor (H)	R14	00h	00h	00h
Cursor (L)	R15	00h	00h	00h

Table 5.2-2 6845 Monochrome/Hercules CRT Controller Registers, Functions and Parameters

Register	Register Number	TEXT 80 x 25	Hercules 720 x 348
Horizontal Total	R0	61h	38h
Horizontal Displayed	R1	50h	2Dh
Hsync Position	R2	52h	2Eh
Hsync Width*	R3	OFh	07h
Vertical Total	R4	19h	5Bh
Vertical Adjust	R5	06h	02h
Vertical Displayed	R6	19h	57h
Vsync Position	R7	19h	57h
Interlace Mode	R8	02h	02h
Max. Scan Line Addr.	R9	0Dh	03h
Cursor Start	R10	0Bh	00h
Cursor End	R11	0Ch	00h
Start Address (H)	R12	00h	00h
Start Address (L)	R13	00h	00h
Cursor (H)	R14	00h	00h
Cursor (L)	R15	00h	00h

*Bit 4, during 6845 CRTC mode operation, defines the vertical synchronous output pulse width as either sixteen lines wide (bit 4=0) or two line wide (bit 4=1).

Register descriptions for the 6845 can be found in the register description pages of Motorola and Hitachi chip product catalogs.

5.3 CRTC Register Description

The CPU interface to the ET4000/W32 internal primary CRT Controller (CRTC) consists of 33 read/write registers. Of these registers, one Register, the CRTC Index Register, is accessed by a separate independent I/O address (3#4, where # = B in monochrome emulation modes; D in color emulation modes, as controlled by bit 0 in the Miscellaneous Output Register.) The remaining 32 registers are internally indexed, which means that they are accessed via a common I/O address (3#5) with one of the 32 registers that is actually accessed selected by the CRTC Index Register.

All values are in hexadecimal unless otherwise noted.

Table 5.3-1 CRTC Index Register

Register Name		Port Address
CRTC Index Register	(Read/Write)	3#4

Table 5.3-2 CRTC Indexed Registers

CRTC Indexed Register Name	CRTC Indexed Address		Port Address
Horizontal Total	0	(Read/Write)	3#5
Horizontal Display End	1	(Read/Write)	3#5
Horizontal Blank Start	2	(Read/Write)	3#5
Horizontal Blank End	3	(Read/Write)	3#5
Horizontal Sync Start	4	(Read/Write)	3#5
Horizontal Sync End	5	(Read/Write)	3#5
Vertical Total	6	(Read/Write)	3#5
Overflow Low	7	(Read/Write)	3#5
Initial Row Addr (Raster Counter)	8	(Read/Write)	3#5
Maximum Row Address	9	(Read/Write)	3#5
Cursor Start Row Address	A	(Read/Write)	3#5
Cursor End Row Address	B	(Read/Write)	3#5
Linear Starting Address Middle	C	(Read/Write)	3#5
Linear Starting Address Low	D	(Read/Write)	3#5
Cursor Address Middle	E	(Read/Write)	3#5
Cursor Address Low	F	(Read/Write)	3#5
Vertical Sync Start	10	(Read/Write)	3#5
Vertical Sync End	11	(Read/Write)	3#5
Vertical Display End	12	(Read/Write)	3#5
Row Offset	13	(Read/Write)	3#5
Underline Row Address	14	(Read/Write)	3#5
Vertical Blank Start	15	(Read/Write)	3#5
Vertical Blank End	16	(Read/Write)	3#5
CRTC Mode	17	(Read/Write)	3#5
Split Scr Start Low (Line Compare)	18	(Read/Write)	3#5
RAS/CAS Configuration	32	(Read/Write)	3#5
Extended Start Address	33	(Read/Write)	3#5
6845 Compatibility Control	34	(Read/Write)	3#5
Overflow High	35	(Read/Write)	3#5
Video System configuration 1	36	(Read/Write)	3#5
Video System configuration 2	37	(Read/Write)	3#5
Horizontal Overflow	3F	(Read/Write)	3#5

= B in monochrome emulation modes, D in color emulation modes, controlled by bit 0 in the Miscellaneous Output Register.

NOTE: The "KEY" must be set in order to write CRTC indices above 18, except indices 33 and 35. (CRTC 35 is protected by bit 7 of CRTC 11). See Section 5.1.2, Input Status Register Zero for definition of "KEY".

Many of the CRTC values, such as the Linear Starting Address and the Vertical Sync Start, are broken up into numerous non-adjacent registers. This is because of the need to maintain IBM VGA and EGA compatibility. For example, vertical sync start bits 7:0 are in Register 10 hex, Vertical Sync Start Bits 9:8 are in Register 7, Overflow Low. These two registers provide the 10-bit vertical sync start value in IBM's VGA. The ET4000/W32 chip supports 11-bit vertical values, so Register 35 hex, Overflow High, contains bit 10 of the vertical sync start value. Although this can sometimes be awkward, it is the only way to provide both IBM VGA and EGA compatibility and the extended functionality of the ET4000/W32 chip.

Because there are so many ET4000/W32 registers and because many CRTC values are spread over numerous registers, the following table lists many of the registers arranged according to general function.

Table 5.3-3 CRTC Registers By Function

Primary Function	Sub Function	CRTC Index	Indexed Register Name
Horizontal timings	Scan line length	0	Horizontal Total (bit 7:0)
		3F	Horizontal Overflow (bit 8)
	Display enable	1 *	Horizontal Display End (bit 7:0)
		3	Horizontal Blank End (bit 6:5)
			(Horizontal Display Enable Skew)
	Blanking	2	Horizontal Blank Start (bit 7:0)
		3F	Horizontal Overflow (bit 8)
		3	Horizontal Blank End (HBE bit 0:4)
		5	Horizontal Sync End (HBE bit 5)
	Sync	4	Horizontal Sync Start (bit 7:0)
		3F	Horizontal Overflow (bit 8)
		5	Horizontal Sync End (bit 4:0)
Vertical timings	Frame height	6	Vertical Total (bit 7:0)
		7	Overflow Low (VT bit 8,9)
		35	Overflow High (VT bit 10)
	Display enable	12	Vertical Display End (bit 7:0)
		7	Overflow Low (VDE bit 8,9)
		35	Overflow High (VDE bit 10)
	Blanking	15	Vertical Blank Start (bit 7:0)
		7	Overflow Low (VBS bit 8)
		9	Maximum Row Address (VBS bit 9)
		35	Overflow High (VBS bit 10)
		16	Vertical Blank End (bit 7:0)
	Sync	10	Vertical Sync Start (bit 7:0)
		7	Overflow Low (VSS bit 8,9)
		35	Overflow High (VSS bit 10)
		11	Vertical Sync End (bit 3:0)
Cursor	Address	F	Cursor Address Low (bit 7:0)
		E	Cursor Address Middle (bit 15:8)
		33	Extended Start Address (CURA bit 19:16)
	Row Address	A	Cursor Start Row Address (bit 4:0)
		B	Cursor Stop Row Address (bit 4:0)
	Skew	B	Cursor Stop Row Address (bit 6,5)
Memory address	Linear address	D	Linear Start Addr Low (bit 7:0)
		C	Linear Start Addr Middle (bit 15:8)
		33	Extended Start Address (LA bit 19:16)
	Row offset	13	Row Offset (bit 7:0)
		3F	Row Offset (bit 8)
Split screen	Start scan line	9	Maximum Row Addr (Split Scr bit 9)
		18	Line Compare (bit 7:0)
		7	Overflow Low (Line Compare bit 8)
		35	Overflow High (Line Compare bit 10)

For the rest of the descriptions in this section, * = B in monochrome emulation modes, D in color emulation modes, controlled by bit 0 of the Miscellaneous Output Register.

5.3.1 CRTC Index

I/O address = 3#4

Bit	Description	Access
7:6	Reserved.	
5:0	Current CRTC index.	RW

Bit	Description
Bits 5:0	These bits provide the index of the currently selected internally indexed register. The CRTC Index register determines which CRTC indexed register will be accessed when a read/write is performed using port address 3#5.

5.3.2 CRTC Indexed Registers

The following registers are CRTC indexed registers. These registers are accessed by first writing the index of the desired register to the CRTC Index register and then accessing the register using the address 3#5.

5.3.3 CRTC Indexed Register 0: Horizontal Total

I/O address = 3#5

Bit	Description	Access
7:0	Total character times per horizontal scan line (-5 VGA, -2 for EGA mode).	RW

Bit	Description
Bit 7:0	The Horizontal Total register defines the horizontal scan line time by controlling the length of the scan line in character times units. The character time unit is defined by TS Indexed Register 1, bit 0.

5.3.4 CRTC Indexed Register 1: Horizontal Display End

I/O address = 3#5

Bit	Description	Access
7:0	Character count of horizontal display enable end -1.	RW

Bit	Description
Bit 7:0	The Horizontal Display End register contains the 8 bit value of the internal horizontal character counter after which the horizontal display enable period is to end. The total number of characters displayed per horizontal scan line is one greater than the contents of the Horizontal Display End register.

5.3.5 CRTC Indexed Register 2: Horizontal Blank Start

I/O address = 3#5

Bit	Description	Access
7:0	Character count of horizontal blanking start.	RW

Bit	Description
Bit 7:0	The Horizontal Blank Start register contains the 8 bit value of the internal horizontal character counter at which horizontal blanking is to start.

5.3.6 CRTC Indexed Register 3: Horizontal Blank End
I/O address = 3#5

Bit	Description	Access
7	Test bit.	RW
6:5	Display enable skew.	RW
4:0	Character count of horizontal blanking end modulo 32 (EGA); 5 least significant bits of character count of horizontal blanking end modulo 64 (VGA mode).	RW

Bit	Description
Bit 7	1 = normal mode of operation.

Bits 6:5 These bits form a 2-bit integer that defines the skew of the horizontal display enable in character clocks as follows.

Bit 6	Bit 5	Skew
0	0	0 character clocks.
0	1	1 character clock.
1	0	2 character clocks.
1	1	3 character clocks.

Bits 4:0 EGA mode: Provides the 5-bit value of the internal horizontal character counter at which horizontal blanking is to end. Since the character counter is an 8-bit counter and the Horizontal Blank End is a 5-bit register, the upper 3 bits of the character counter are ignored in making this comparison. This means that the horizontal blanking end position is defined relative to the horizontal blanking start position; the first time after the start of horizontal blanking that the Horizontal Blank End register matches the lower 5 bits of the character counter, horizontal blanking will end.

VGA mode: The Horizontal Blank End register value is increased to six bits; the five bits will provide the least significant five bits of this value, while the most significant bit is found in CRTC Indexed Register 5 (Horizontal Sync End register) bit 7.

5.3.7 CRTC Indexed Register 4: Horizontal Sync Start
I/O address = 3#5

Bit	Description	Access
7:0	Character count of horizontal sync start.	RW

Bit	Description
Bits 7:0	The Horizontal Sync Start register contains the 8-bit value of the internal horizontal character counter at which horizontal sync (the horizontal retrace pulse) is to start.

5.3.8 CRTC Indexed Register 5: Horizontal Sync End
I/O address = 3#5

Bit	Description	Access
7	Bit 5 of Horizontal Blank End for VGA modes.	RW
6:5	Horizontal sync skew.	RW
4:0	Character count of horizontal sync end modulo 32.	RW

Bit	Description
Bit 7	Provides bit 5 of the Horizontal Blank End value for VGA modes.

Bits 6:5 These bits form a 2-bit integer that defines the skew of the horizontal sync signal in character clocks as follows:

Bit 6	Bit 5	Skew
0	0	0 character clocks.
0	1	1 character clock.
1	0	2 character clocks.
1	1	3 character clocks.

Bits 4:0 These bits make up the 5-bit value of the internal horizontal character counter at which horizontal sync is to end. Since the character counter is an 8-bit counter and horizontal sync end is a 5-bit value, the upper three bits of the character counter are ignored in making this comparison. This means that the horizontal sync end position is defined relative to the horizontal sync start position; the first time after the start of horizontal sync that the Horizontal Sync End register matches the lower 5 bits of the character counter, horizontal sync will end.

5.3.9 CRTC Indexed Register 6: Vertical Total
I/O address = 3#5

Bit	Description	Access
7:0	VGA mode: Horizontal scan lines per vertical frame -2 (bits 7:0).	RW
	EGA Mode: Horizontal scan lines per vertical frame -1 (bits 7:0).	RW

Bit	Description
Bits 7:0	The Vertical Total register contains the lower eight bits of the 11-bit vertical total value, which defines the number of horizontal scan lines per vertical frame. Note that bits 9:8 of the vertical total value are in the Overflow Low register, and bit 10 is in the Overflow High register.

5.3.10 CRTC Indexed Register 7: Overflow Low
I/O address = 3#5

Bit	Description	Access
7	Vertical Sync Start (bit 9).	RW
6	Vertical Display Enable End (bit 9).	RW
5	Vertical Total (bit 9).	RW
4	Line Compare (Split Screen) (bit 8).	RW
3	Vertical Blank Start (bit 8).	RW
2	Vertical Sync Start (bit 8).	RW
1	Vertical Display Enable End (bit 8).	RW
0	Vertical Total (bit 8).	RW

Bit	Description
Bits 7:0	The Overflow register contains one extra bit for each of five values that cannot fit in a single byte. Bits 9:8 of the Vertical Total, Vertical Display Enable End, and Vertical Sync Start are contained in the Overflow register, as is bit 8 for Vertical Blank Start and Line Compare.

5.3.11 CRTC Indexed Register 8: Preset Row Scan/Initial Row Address
I/O address = 3#5

Bit	Description	Access
7	Reserved.	
6:5	Byte Panning.	RW
4:0	Initial row address after vertical sync.	RW

To access this register in 6845 compatibility mode, use CRTC Indexed Register 35 for the register address (instead of CRTC Indexed Register 8).

Bit	Description
Bits 4:0	Define he row address of the first scan line following vertical sync.
Bits 6:5	Control horizontal byte panning in modes programmed as multiple shift modes.

5.3.12 CRTC Indexed Register 9: Maximum Row Address
I/O address = 3#5

Bit	Description	Access
7	Double Scan Enable: 200-to-400 scan line conversion.	RW
6	Line Compare (Split Screen) bit 9.	RW
5	Vertical Blank Start bit 9 .	RW
4:0	Number of scan lines per character row -1.	RW

Bit	Description
Bit 7	When set to 1, sets scan lines to 400 from 200. This divides the clock in the row scan counter by 2, effectively doubling the lines displayed by displaying every line twice. When set to 0, returns the row scan counter clock equal to the horizontal scan rate
Bit 6	Bit 9 of the Line Compare (Split Screen) register.
Bit 5	Bit 9 of the Vertical Blank register.
Bits 4:0	These bits define the height in scan lines of each character row. It is used to select the desired scan line from the font character being displayed

5.3.13 CRTC Indexed Register A: Cursor Start Row Address
I/O address = 3#5

Bit	Description	Access
7	Reserved.	
6	Reserved.	
5	Used to turn the cursor off (=1) or on (=0).	RW
4:0	The row address at which the cursor starts being enabled.	RW

Bit	Description
Bit 5	When set to 1, turns the cursor off. When set to 0, turns the cursor on.
Bits 4:0	These bits contain the value of the internal row address counter at which the cursor is to begin to be enabled.

5.3.14 CRTC Indexed Register B: Cursor End Row Addres

I/O address = 3#5

Bit	Description	Access
7	Reserved.	
6:5	Cursor skew.	RW
4:0	The row address at which the cursor stops being enabled.	RW

Bit **Description**

Bits 4:0 These bits contain the row address at which the cursor is to stop being enabled. That is, Cursor End Row Address register = last cursor row address displayed + 1

Bits 6:5 These bits form a 2-bit integer that defines the skew of the cursor signal in character clocks as follows:

Bit 6	Bit 5	Skew
0	0	0 character clocks.
0	1	1 character clock.
1	0	2 character clocks.
1	1	3 character clocks.

In general, the cursor location must maintain a relationship with the display enable signal such that a cursor positioned at both the extreme left and extreme right of the screen will always appear.

5.3.15 CRTC Indexed Register C: Linear Starting Address Middle

I/O address = 3#5

Bit	Description	Access
7:0	Linear starting address (<15:8>).	RW

Bit **Description**

Bits 7:0 This register contains bits 15:8 of the 20-bit linear starting address. The linear starting address is the display memory address at which the regen buffer (the area of memory scanned by the linear counter for video data) begins; the linear counter is set to this value at the start of the vertical frame. The linear starting address can be incremented or decremented to perform horizontal character panning; the ATC's horizontal pixel panning feature can be used for finer horizontal panning. In graphics modes, the linear starting address can be incremented or decremented by the value of the Row Offset register to perform smooth (scan line) vertical scrolling. In text modes, the linear starting address can be used to perform character vertical scrolling; in this case, the Initial Row Address register can be used to adjust, on a scan line basis, to smooth- scroll the text.

Note that bits 19:16 of the linear starting address are in the Extended Start Address register and bits 7:0 are in the Linear Starting Address Low register.

5.3.16 CRTC Indexed Register D: Linear Starting Address Low

I/O address = 3#5

Bit	Description	Access
7:0	Linear starting address (<7:0>).	RW

Bit **Description**

Bits 7:0 This register contains bits 7:0 of the 20-bit linear starting address. See Section 5.3.15, Linear Starting Address Middle register for details on the linear starting address.

5.3.17 CRTC Indexed Register E: Cursor Address Middle

I/O address = 3#5

Bit	Description	Access
7:0	Cursor start address (<15:8>).	RW

Bit **Description**

Bits 7:0 This register contains bits 15:8 of the 20-bit cursor address. The cursor address is the display memory address at which the cursor is located in text mode.

Note that bits 7:0 of the cursor address are in the Cursor Address Low register, and bit 19. 16 are in the Extended Start Address Register (See Section 5.3.20).

5.3.18 CRTC Indexed Register F: Cursor Address Low

I/O address = 3#5

Bit	Description	Access
7:0	Cursor start address (<7:0>).	RW

Bit **Description**

Bits 7:0 The Cursor Address Low register contains bits 7:0 of the 20-bit cursor address. See Section 5.3.17, Cursor Address Middle register for details on the cursor address.

5.3.19 CRTC Indexed Register 10: Vertical Sync Start
I/O address = 3#5

Bit	Description	Access
7:0	Scan line at which vertical sync starts.	RW

Bit	Description
Bits 7:0	This register contains the lower eight bits of the 11-bit vertical sync start value. The vertical sync start value specifies the value of the internal line counter at which vertical sync (the vertical retrace pulse) is to start. Note that bits 9:8 of the vertical sync start value are in the Overflow Low register, and bit 10 is in the Overflow High register.

5.3.20 CRTC Indexed Register 11: Vertical Sync End
I/O address = 3#5

Bit	Description	Access
7	Protection bit.	RW
6	Reserved.	
5	Enable vertical interrupt when low	RW
4	Clear vertical interrupt when low.	RW
0-3	Scan line at which vertical sync ends modulo 16.	RW

Bit	Description
Bit 7	When set to 1, prevents CRTC registers 0-7 and 35, from being written to, with the exception of bit 4 of the Overflow register (CRTC Register 7) and bits 4,7 of CRTC Indexed Register 35
Bit 5	When set to 0, enables the vertical interrupt to occur. If bit 5 is set to 0 and the vertical interrupt is cleared, then IRQ will be asserted when "VS" becomes true. When set to 1, vertical interrupts cannot occur.
Bit 4	When set to 0, clears the vertical interrupt. If bit 5 is low and the vertical interrupt is cleared, then output pin IRQ will be asserted when output line "VS" becomes true. The vertical interrupt should be cleared whenever a vertical interrupt occurs, before re-enabling interrupts.
Bits 3:0	These bits contain the 4-bit value of the internal line counter at which the vertical sync signal is to end. Since the line counter is an 11-bit counter and vertical sync end is a 4-bit value, the upper 7 bits of the line counter are ignored in making this comparison. This means that the vertical sync end position is defined relative to the vertical sync start position; the first time after the start of vertical sync that the Vertical Sync End register matches the lower 4 bits of the line counter, vertical sync will end.

5.3.21 CRTC Indexed Register 12: Vertical Display End
I/O address = 3#5

Bit	Description	Access
7:0	Number of last scan line displayed vertically.	RW

Bit	Description
Bits 7:0	This register contains the lower eight bits of the 11-bit vertical display end value. Note that bits 9:8 of the vertical display end value are in the Overflow Low register, while bit 10 is in the Overflow High register.

5.3.22 CRTC Indexed Register 13: Row Offset
I/O address = 3#5

Bit	Description	Access
7:0	Word memory address offset between the start of one displayed row and the next.	RW

Bit	Description
Bits 7:0	This register specifies the amount to be added to the internal linear counter when advancing from one screen row to the next. The addition is performed whenever the internal row address counter advances past the maximum row address value, indicating that all the scan lines in the present row have been displayed. The Row Offset register is programmed in terms of CPU-addressed words per scan line, counted as either words or doublewords, depending on whether byte or word mode is in effect. If the CRTC Mode register is set to select byte mode, the Row Offset register is programmed with a word value, so for a 640-pixel (80-byte) wide graphics display, a value of 80/2 = 40 (28 hex) would normally be programmed, where 80 is the number of bytes per scan line. If the CRTC Mode register is set to select word mode, then the Row Offset register is programmed with a doubleword, rather than a word, value. For instance, in 80 column text mode, a value of 160/4=40 (28 hex) would be programmed, because from the CPU-addressing side, each character requires 2 linear bytes (character code byte and attribute byte), for a total of 160 (A0 hex) bytes per row. In effect, the Row Offset register defines a virtual screen width, so that the physical screen area could be considered a window onto a virtual screen that has a width defined by the Row Offset register. The horizontal pixel panning feature of the ATC can be used with the linear start address to move horizontally around a virtual screen larger than the actual screen size, and the linear start address and the Initial Row Address register can be used to move vertically.

5.3.23 CRTC Indexed Register 14: Underline Row Address
I/O address = 3#5

Bit	Description	Access
7	Reserved (=0).	
6	Doubleword addressing.	RW
5	Linear address count by 4.	RW
4:0	Row address at which underline signal is to be asserted.	RW

Bit	Description
Bit 6	When set to 1, indicates that memory addresses being used are doubleword addresses.
Bit 5	When set to 1, clocks the memory address counter with the character clock divided by 4, used when doubleword addressing is used. NOTE: When bit 3 of the CRTC Mode Register also = 1, the linear counter will increment twice per character.
Bits 4:0	These bits contain the value of the row address counter at which the underline is to be enabled. The ATC enables underline attribute decoding and displays the underline whenever the underline attribute is true during that scan line. The underline may be disabled by setting the Underline Row Address register to a value greater than the setting of the Maximum Row Address register. The value set is equal to the scan line number requested minus one.

5.3.24 CRTC Indexed Register 15: Vertical Blank Start
I/O address = 3#5

Bit	Description	Access
7:0	Scan line at which vertical blanking begins -1.	RW

Bit	Description
Bits 7:0	This register contains bits 7:0 of the 11-bit Vertical Blank Start value. The Vertical Blank Start specifies the value of the internal line counter at which vertical blanking is to start -1. Note that bit 8 of the Vertical Blank Start value is in the Overflow Low register, and bit 9 of the Vertical Blank Start value is in the Maximum Row Address register, while bit 10 is in the Overflow High register.

5.3.25 CRTC Indexed Register 16: Vertical Blank End
I/O address = 3#5

Bit	Description	Access
7:0	Scan line at which vertical blanking ends.	RW

Bit	Description
Bits 7:0	This register contain the 8-bit value of the internal line counter at which vertical blanking is to end. Since the line counter is an 11-bit counter and the Vertical Blank End is a 8-bit register, the upper three bits of the line counter are ignored in making this comparison. This means that the vertical blanking end position is defined relative to the Vertical Blanking Start position; the first time after the start of vertical blanking that the Vertical Blank End register matches the lower 8 bits (In EGA mode only bits 4.0 are used in the comparison) of the line counter, vertical blanking will end.

5.3.26 CRTC Indexed Register 17: CRTC Mode
I/O address = 3#5

Bit	Description	Access
7	Hold control.	RW
6	Word/byte mode select.	RW
5	Alternate address line +MA00 output.	RW
4	Reserved.	RW
3	Linear counters count by 2.	RW
2	Line counter count by 2.	RW
1	Alternate address line LA14 output.	RW
0	Alternate address line LA13 output.	RW

Bit	Description
Bit 7	When set to 0, places all horizontal and vertical timing control circuitry into a hold state.
Bit 6	When set to 0, selects word mode. When set to 1, selects byte mode.
Bit 5	Provides an alternate value for LA00 output during the display enable period, that is, the display memory address line LA00 is multiplexed. In word mode, when this bit is set to 0, the LA00 output line is equal to linear counter bit 15. When this bit is set to 1, the LA00 output line is equal to linear counter bit 15. In byte mode, bit 5 has no effect, and linear counter bit 0 is always multiplexed to LA00. Word mode is typically used in text mode. The reason for selecting this alternate value for LA00 is so that the CRTC display memory mapping matches the CPU display memory mapping. In text mode, even/odd mode (See Section 5.4.7, TS Memory Mode register) is active to allow CPU memory addressing to match the CRTC organization of display memory. In even/odd mode, the CPU A<0> line is used to select between plane 0 and plane 1, with planes 2 and 3 storing the soft character font. The CRTC matches this by shifting the linear address counter up one bit before placing it on the LA(17:00) lines (refer to the discussion of bit 6, word/byte mode select, below), and then the full 16 bits of the character code and attribute for a given character are accessed in parallel to generate the character. Consequently, the linear counter provides no direct value for the LA00 line. The highest useful linear address counter value should be wrapped to LA00, to provide the maximum addressable memory in text modes. When

16KB per plane is installed, bit 5 should be set to 0 to wrap linear address bit 13 to LA00, providing the CRTC with 16KB addressing. When more than 16KB of memory per plane is installed, bit 5 should be set to 1 to wrap linear address bit 15 to LA00, providing the CRTC with 64KB of addressing.

Externally, the CPU address line A<14> or A<16> or a page select bit, should correspond to the LA00 line in even/odd mode. In non-even/odd mode, the CPU address line A<0> should correspond to the LA00 line.

Bit 3 — When set to 1, causes the linear counter to increment on every other character clock, rather than incrementing on every character clock.

When set to 0, the linear counter is incremented on every character clock. This is typically associated with situations where DOTCLK is not divided by two but VLOAD is divided by two and word mode addressing is selected; the linear counting is divided by two to synchronize the linear counters with the ATC video data rate. If VLOAD and DOTCLK are both divided by two, then bit 3 should not be set to 1. NOTE: When this bit = 1 and bit 5 of the Underline Row Address Register also = 1, then the linear counter will increment twice per character.

Bit 2 — When set to 1, causes the line counter to increment on every other scan line, rather than incrementing on every scan line. This has the effect of doubling all vertical timings without affecting any horizontal timings.

When set to 0, the line counter increments with every scan line.

Bit 1 — Provides an alternate value for LA14 output during the display enable period; that is, the display memory address line LA14 is multiplexed.

When bit 1 is set to 1, linear counter bit 14 or bit 13, in byte or word mode, respectively, is multiplexed to LA14.

When this bit is set to 0, the LA14 output line is equal to row address bit 1, so that out of each group of four scan lines, scan lines 2 and 3 are addressed 16KB after the corresponding even scan lines 0 and 1.

Bit 0 — Provides an alternate value for LA13 output during the display enable period; that is, the display memory address line, LA13, is multiplexed.

When bit 0 is set to 1, linear counter bit 13 or bit 12, in byte or word mode, respectively, is multiplexed to LA13.

When this bit is set to 0, the LA13 output line is equal to row address bit 0, so each odd scan line is addressed 8KB after the corresponding even scan line. This is used to emulate the 6845 CRT Controller used in the IBM Color/Graphics Adapter.

5.3.27 CRTC Indexed Register 18: Line Compare (Split Screen)

I/O address = 3#5

Bit	Description	Access
7:0	Line Compare.	RW

Bit — **Description**

Bits 7:0 — This register contains bits 7:0 of the compare target. The line compare target value specifies the value of the internal line counter at which the internal linear counter is to be reset to 0. This means that at the scan line after the scan line specified by the line compare target value the display will reflect the contents of display memory starting at address 0. This split screen section will continue to the bottom of the screen, and will remain unchanged even if the linear starting address is changed.

Note that bit 8 of the line compare value is contained in the Overflow Low register, bit 9 is in the Maximum Row Address register, while bit 10 is in the Overflow High register.

The following CRTC registers are TLI's extended registers. To write to these register(s) (except indices 33 and 35), the "KEY" must be set. (CRTC Indexed Register 35 is protected by bit 7 of CRTC 11.) See Section 5.1.2, Input Status Register Zero for definition of "KEY".

5.3.28 CRTC Indexed Register 30: System Segment Map Comparator

I/O address = 3#5

Bit	Description	Access
7:5	Reserved.	
4:0	Addressing mode.	RW

Bit — **Description**

Bits 4:0 — These bits are compared to the host's upper address bus or decode and are used to select the video memory segments within the system memory map. The default value on power-up for bits 4:0 is

Bits
4 3 2 1 0
1 1 1 0 0

ISA bus bits 1:0 compare to inputs SEGE and A<22>, respectively. If System Linear Mode is disabled, this comparison is ANDed with inputs A<21> and A<20>, which must be low. If System Linear Mode is enabled, A<21> and A<20> are address inputs. Bits 4:2 are always ignored.

MCA bus bits 2:0 compare to inputs MADE24, A<23> and A<22>, respectively. If System Linear Mode is disabled, this comparison is ANDed with inputs A<21> and A<20>, which must be low. If System Linear Mode is enabled, A<21> and A<20> are address inputs. Bits 4:3 are always ignored.

Local Bus bits 5:0 compare to inputs SEG2, SEG1, SEG0, A<23>, and A<22>, respectively. If System Linear Mode is disabled, this comparison is ANDed with inputs A<21> and A<20>, which must be low. If System Linear Mode is enabled, A<21> and A<20> are address inputs.

When the Image Port is enabled, A<22:20> are ignored (see Section 5.8, IMA Register Descriptions, and 3.8, Image Port Interface). Consequently, maximum system linear space is 1MB.

5.3.29 CRTC Indexed Register 31: General Purpose

I/O address = 3#5

Bit	Description	Access
7	Clock Select 4.	RW
6	Clock Select 3.	RW
5:4	Reserved.	
3:0	General purpose.	RW

Bit **Description**

Bits 3:0 These bits are provided to the programmer as a general storage location. An example of its use would be to maintain configuration information about the video system.

Bits 6:7 The values in these bits are driven out on the CS<4> and CS<3> pins (see Section 3.4). Clock Select bit 2 is in the CRTC Indexed Register 34, bit 6, and Clock Select bits <1:0> are in Miscellaneous Output Register, bits <3:2>. These five clock select lines provide selection of up to 32 different video clock frequencies.

5.3.30 CRTC Indexed Register 32: RAS/CAS Configuration (RCCONF; protected by key)

I/O address = 3#5

Bit	Description	Access
7	Reserved.	
6	RAL RAS & CAS column setup time.	RW
5	RCD RAS to CAS time, 1=3 clock, 0=2 clock.	RW
4:3	RSP<1:0> ($1+2)*SCLK, RAS pre-charge time.	RW
2	CSP<0> ($1+1)*SCLK, CAS pre-charge time.	RW
1:0	CSW<1:0> ($1+1)*SCLK, CAS low pulse-width.	RW

Bit **Description**

Bit 6 Provides 1-bit column address hold time control (Tral). When set to 1, an additional SCLK clock period will be added to the RAS low pulse width and to the last CAS low pulse width of each RAS cycle. This will effectively increase the column address hold time by one additional SCLK clock period. Note that the RAS pre-charge time will be reduced by one SCLK clock period.

NOTE: 1. The RAS low pulse width is equal to Trcd + n(Tcsw) + (n-1)Tcsp + Tral, where n is number of CAS cycles.

2. The RAS high pulse width is equal to Trsp - Tral.

Bit 5 When set to 1, causes the Trcd time to be equal to 3 SCLK clock periods. When set to 0, the Trcd time is reduced to 2 SCLK periods.

Bits 4:3 RSP<1:0>, plus 2, form a programmed value for RASB, RASA pre-charge control (Trsp). The actual pulse width high is equal to the programmed value plus 2 of SCLK clock period.

Bit 2 CSP<0>, plus 1 ($1+1), is the 1-bit programmed value for CAS<3:0> pre-charge control (Tcsp). The actual pulse width high is equal to the programmed value plus 1 of SCLK clock period.

Bits 1:0 CSW<1:0>, plus 1 ($1+1), form the programmed value for low CAS pulse width control (Tcas). The actual pulse width value in SCLK periods is determined by the following table:

CRTC 32

Mode CSW <1:0>	Graphics CAS<3:0> CAS Low Pulse Width	Text CAS<3:2> CAS Low Pulse Width	CAS<1:0> CAS Low Pulse Width
0 0	1	1	1
0 1	2	2	2
1 0	3	3	3
1 1	4	4	4

5.3.31 CRTC Indexed Register 33: Extended Start Address
I/O address = 3#5

Bit	Description	Access
7:4	Cursor address bit (<19:16>).	RW
3:0	Linear start address bits (<19:16>).	RW

Bit	Description
Bits 7:4	These are bits 19:16 of the 20-bit Cursor Address value.
Bits 3:0	These are bits 19:16 of the 20-bit Linear Starting Address value.

5.3.32 CRTC Indexed Register 34: 6845 Compatibility Control Register (protected by key)
I/O address = 3#5

Bit	Description	Access
7	6845 1=enable 6845 compatibility.	RW
6	ENBA 1=enable double scan/underline in AT&T compatible mode.	RW
5	ENXL 1=enable translation ROM when writing CRTC/MISCOUT.	RW
4	ENXR 1=enable translation ROM when reading CRTC/MISCOUT.	RW
3	ENVS VSE register port address (1=46E8, 0=3C3).	RW
2	TRIS 1=tri-state the ET4000/W32's output tri-state pins.	RW
1	CS2 MCLK clock select 2*	RW
0	EMCK 1=enable translation of CS0 bit.	RW

Bit	Description
Bit 7	When set to 1, enables 6845 compatibility. Several steps need to be taken in order to program for 6845 compatibility. The ET4000/W32 internal registers should be programmed as follows in order to fully emulate the IBM CGA/MDA or Hercules modes: A. Load the font and set the external palette appropriately for the mode to be selected 1. color: set 200-scan line mode 3 first to load font, set external palette. 2. mono: set 350-scan line mode 7 first to load font, set external palette. B. Set the appropriate EGA/VGA table for the correct mode (See Table 5.3-5).* C. Set bit 7 of the CRTC Indexed Register 34 for CGA/MDA/Hercules compatibility.** D. Set the appropriate Display Mode Control register (3#8). E. Program the 6845 CRTC registers (3#4, 3#5) for the compatibility mode to be selected (CGA/MDA/Hercules). (In color mode, also set the color register (3D9).)

* Note that the values programmed into the Miscellaneous Output Register and TS Indexed Register 7 (relating to the clock and sync polarities) can vary depending on the adapter's clock configuration, whether or not translation is enabled, and the target monitor. The ROM configuration also affects TS Indexed Register 7.

** Other bits in CRTC Indexed Register 34, in addition to bit 0 of the AT&T Mode Control Register ((3DE) for double scan)
may also need to be set depending on the target monitor and whether or not translation is enabled.

A driver is needed to select for EGA/VGA modes, and, to in turn, select for 6845 monochrome, or 6845 color compatibility.

Bit 6	When set to 1, enables the double scan and underline color attributes. (See Section 5.2.4, AT&T Mode Control Register.)
Bits 5 4	(Bit 5 for write, bit 4 for read) when set to 1, disable the RDMEL output when an I/O read/write to the CRTC Data register 3#5 or MISCOUT register is performed. This allows the external translation ROM to be enabled for the CRTC register. To use the translation, external ROM must be incorporated. When set to 0, the Translation Mode is disabled.
Bit 3	When set to 1, will set the Video Subsystem Enable register port address to 46E8; 0 = 3C3.
Bit 2	When set to 1 (Output tri-state control), causes all output pins to go to a tri-state condition. The symbols are as follows; see Section 3 for pin numbers. RASB*, RASA*, CAS<3:0>*, MWB*, MWA*, MD<31:0>, AB<9:0>, AA<9:0>, VS, HS, AP<7:0>, PCLK, MBS*
Bit 1	Clock select 2 (CS2), in conjunction with the MISCOUT<2:2> clock select lines (CS1, CS0) and in combination with CRTC Indexed Register 31<7:6>, provides up to 32 video clocks to be selected. See CRTC Indexed Register 31 for more information regarding clock selects.
Bit 0	When set to 1, is used to enable the ET4000/W32 to translate the clock select bits (CS1,CS0). (See Section 5.1.1, Miscellaneous Output Register.) Also, during ENXL set to 1, EMCK is used to select the external translation ROM's map while in 6845 mode (see Miscellaneous Output Register).

Table 5.3-5 ET4000/W32 6845 Color Emulation Setup Register Values

Register Name	Port	Index	Mode of Operation CGA	MDA
Misc. Output	3C2	-	37	AA
Timing Sequencer				
TS Index	3C4	-		
Synch Reset	3C5	00	03	03
TS Mode	3C5	01	00	00
Write Plane Msk	3C5	02	03	03
Font Select	3C5	03	00	00
Memory Mode	3C5	04	02	02
Reserved	3C5	05		
State Control	3C5	06	00	00
TS Aux Mode	3C5	07	48	48

CRT Controller Registers

Register Name	Port	Index	Mode of Operation CGA	MDA
CRTC Index	3D4	-		
Horiz Tot	3D5	00	50	50
Hor Dis End	3D5	01	00	00
Hor Blnk Strt	3D5	02	00	00
Hor Blnk End	3D5	03	20	20
Hor Sync Strt	3D5	04	00	00
Hor Sync End	3D5	05	60	20
Vert Tot	3D5	06	F0	F0
Overflow Low	3D5	07	10	10
Init Row Addr	3D5	08	00	00
Max Row Addr	3D5	09	00	00
Cursor Strt	3D5	0A	00	00
Cursor End	3D5	0B	00	00
Lin Strt Mid	3D5	0C	00	00
Lin Strt Low	3D5	0D	00	00
Cursor Mid	3D5	0E	00	00
Cursor Low	3D5	0F	00	00
Vrt Sync Strt	3D5	10	00	00
Vrt Sync End	3D5	11	20	20
Vrt Dis End	3D5	12	00	00
Row Offset	3D5	13	00	00
Underline Row	3D5	14	1F	0D
Vrt Blnk Strt	3D5	15	00	00
Vrt Blnk End	3D5	16	00	00
CRTC Mode	3D5	17	A0	A0
Line Compare	3D5	18	FF	FF
Ext'd Strt Add	3D5	33	00	00
Overflow Hi	3D5	35	00	00

GDC Registers

Register Name	Port	Index	Mode of Operation CGA	MDA
GDC Index	3CE			
Set/Reset	3CF	00	00	00
Enabl Set/Res	3CF	01	00	00
Colr Compare	3CF	02	00	00
Data Rotate	3CF	03	00	00
Read Plane Sel	3CF	04	00	00
GDC Mode	3CF	05	10	10
Miscellaneous	3CF	06	0E	0A
Color Care	3CF	07	00	00
Bit Mask	3CF	08	FF	FF

ATC Indexed Registers

Register Name	Port	Index	Mode of Operation CGA	MDA
ATC Index	R/W 3C0			
Palette	R:3C1/W:3C0	00	00	00
Palette	R:3C1/W:3C0	01	01	08
Palette	R:3C1/W:3C0	02	02	08
Palette	R:3C1/W:3C0	03	03	08
Palette	R:3C1/W:3C0	04	04	08
Palette	R:3C1/W:3C0	05	05	08
Palette	R:3C1/W:3C0	06	06	08
Palette	R:3C1/W:3C0	07	07	08
Palette	R:3C1/W:3C0	08	10	10
Palette	R:3C1/W:3C0	09	11	18
Palette	R:3C1/W:3C0	0A	12	18
Palette	R:3C1/W:3C0	0B	13	18
Palette	R:3C1/W:3C0	0C	14	18
Palette	R:3C1/W:3C0	0D	15	18
Palette	R:3C1/W:3C0	0E	16	18
Palette	R:3C1/W:3C0	0F	17	18
Mode Ctrl	R:3C1/W:3C0	10	00	00
Overscan Clr	R:3C1/W:3C0	11	00	00
Clr Plane En	R:3C1/W:3C0	12	00	00
Hor Pix Pan	R:3C1/W:3C0	13	00	08
Color Select	R:3C1/W:3C0	14	00	00
Miscellaneous	R:3C1/W:3C0	16	00	00

5.3.33 CRTC Indexed Register 35: Overflow High

I/O address = 3#5

Bit	Description	Access
7	Vertical interlace mode (1=enable).	RW
6	CRTCB or CRTC interrupt select.	RW
5	External sync reset (gen-lock) the line/chr counter (1=enable).	RW
4	Line Compare (Split Screen) Bit 10.	RW
3	Vertical Sync Start Bit 10.	RW
2	Vertical Display End Bit 10.	RW
1	Vertical Total Bit 10.	RW
0	Vertical Blank Start Bit 10.	RW

Bit **Description**

Bit 7 When set to 1, will enable the vertical interlace mode where the odd-numbered lines will be displayed, followed by the even-numbered lines, thus doubling the effective vertical resolution with the same vertical timing.

Bit 6 When set to 1, will select the CRTCB or Sprite as the vertical interrupt.

When set to 0, will select the CRTC as the vertical interrupt.

Note: To enable/clear vertical interrupt, see Section 5.3.20, CRTC Indexed Register 11, bits 5:4

Bit 5 When set to 1, will enable the SYNR input to reset the ET4000/W32's internal line and character counter asynchronously. Also, the TKN<1:0> outputs are redefined as TKN<1>= interlace mode active, TKN<0>=EVEN field. For additional details see Section 3, I/O pin descriptions.

Note: SYNR is redefined as Image Port Data Byte Mask if IMAF/IMA Indexed Register F7: Image Port Enable, CRTCB/Sprite Enable, bit 0 is set to 1. See Section 3 I/O Pin Description for an explanation of SYNR.

Bits 4:0 These are bit 10 of the Line Compare (Split Screen Start), Vertical Sync Start, Vertical Display End, Vertical Total, and Vertical Blank Start values, respectively.

5.3.34 CRTC Indexed Register 36: Video System Configuration 1 (VSCONF1) (protected by key)

I/O address = 3#5

Bit	Description	Access
7	16-bit I/O read/write (1=enable).	RW
6	16-bit display memory read/write (1=enable).	RW
5	Enable Memory Mapped Registers.	RW
4	Enable system linear map.	RW
3	Enable Memory Management Buffers.	RW
2:0	Refresh count per line -1.	RW

Bit **Description**

Bit 7 When set to 1 in ISA, Micro Channel, and Local Bus implementations, will enable the 16-bit CPU I/O read/write data bus interface at the DB<15:0> input.

When set to 0 (power-up default condition) in ISA or Micro Channel implementations, will enable the 8-bit CPU I/O read/write data bus interface. For Local Bus implementations, the power-up default is 1.

Bit 6 When set to 1 (power-up default condition) in ISA, Micro Channel, and Local Bus implementations, will enable the 16-bit CPU memory read/write data bus interface at the DB<15:0> input.

When set to 0 in ISA or Micro Channel implementations, will enable the 8-bit CPU memory read/write data bus interface at the DB<15:0> input. For Local Bus implementations, 0 will enable the 32-bit CPU memory read/write data bus interface.

Bit 5 When set to 1 (and bit 3 also set to 1), enables the memory mapped registers (MMU and Accelerator). See Sections 2.10 - 2.11 for more information on memory mapped registers, and Section 7.3 for the effect this bit has on the Video Memory Map.

Bit 4 When set to 1, enables the system linear map, i.e., the video memory is accessed directly as flat CPU addresses in an up to 4 megabyte area of physical memory, rather than via the 64K segments at physical address A0000/B0000.

Bit 3 When set to 1, enables the three memory management buffers. Accessing one of these buffers will indirectly access the video memory at an offset determined by the corresponding MMU Base Pointer register. See Sections 2.10 - 2.11 for more information on memory mapped registers, and Section 7.3 for the effect this bit has on the Video Memory Map.

Bits 2:0 These bits form a 3-bit value equal to the number -1 refresh per CRTC display lines.

5.3.35 CRTC Indexed Register 37: Video System Configuration 2 (VSCONF2) (protected by key)

I/O address = 3#5

Bit	Description	Access
7	Reserved.	
6	Test: 1=TI internal test mode.	RW
5	Priority threshold control (0=more memory BW).	RW
4	16-bit ROM enable.	RW
3	Effective Row/Column memory address (AB<9:0>, AA<9:0>).	RW
2	CAS<3:0>*, MWB*, MWA* definition control.	RW
1	Reserved.	
0	Display Memory data bus width.	RW

Bit **Description**

Bit 6 When set to 1, directs the ET4000/W32 to internal test mode set-up. This bit must set to 0 at all other times for normal operation.

Bit 5 When set to 0, will increase the utilization of the display memory's band-width. However, the memory's response time will also be increased. This bit should normally be set to 0 for better performance.

Bit 4 When set to 1, enables the 16-bit ROM configuration for ISA, Micro Channel, and Local Bus implementations (power-up default for Local Bus). When set to 0, enables the 8-bit ROM configuration for ISA and Micro Channel implementations, and 32-bit for Local Bus. The following table illustrates the configurations:

	16-bit ISA/MCA Bus	32-bit Local Bus
32-bit enable	-	0
16-bit enable	1	1
8-bit enable	0	-
Power-up	0	1

NOTE: If 16-bit ROM is selected with the ISA bus, then the ROM size should be set to 32K. Bits 3 & 5 of TS Indexed Register 7: TS Auxiliary Mode must be set to 1,1 so that the ROM size is set to 32K.

Bit 3 Determines the effective row/column memory address, as illustrated in the following table.

DRAM Type	Programmed Bit 3 value	Row Address	Column Address
256K x 4,8,16	1	AB<8:0>	AB<8:0>
		AA<8:0>	AA<8:0>
512K x 4,8	1	AB<9:0>	AB<8:0>
		AA<9:0>	AA<8:0>
1MB x 4	0	AB<9:0>	AB<9:0>
		AA<9:0>	AA<9:0>

Bit 2

When set to 1 (power-up condition), CAS<3:0>* are the CAS* signals to the Memory with one CAS* signal per byte of data, and, MWB* and MWA* are the WRITE ENABLE* signals to the Memory with one WRITE ENABLE* signal per word (two bytes) of data. This is the Rev. G- compatible mode.

When set to 0, CAS<3:0>* are the WRITE ENABLE* signals to the Memory with one WRITE ENABLE* signal per byte of data, and, MWB* and MWA* are the CAS* signals to the Memory with one CAS* signal per word (two bytes) of data. This is the W32i-compatible mode. See Appendix C for DRAM configuration examples.

The following table helps to illustrate the conditions:

Bit 2=1 (power-up condition) (Rev. G compatibility)				
DRAM Signal	MD<31:24>	MD<23:16>	MD<15:8>	MD<7:0>
CAS*	CAS<3>*	CAS<2>*	CAS<1>*	CAS<0>*
WRITE ENABLE*	MWB*	MWB*	MWA*	MWA*
Bit 2=0 (W32i compatibility)				
DRAM Signal	MD<31:24>	MD<23:16>	MD<15:8>	MD<7:0>
CAS*	MWB*	MWB*	MWA*	MWA*
WRITE ENABLE*	CAS3*	CAS2*	CAS1*	CAS0*

NOTE: The W32i mode allows DRAM to operate in an interleaved fashion. The ET4000/W32i utilizes the interleave capability and uses the 2 CAS* and 4 WRITE ENABLE* signal configuration exclusively. ET4000/W32 designs should be configured in this manner to provide an upgrade path to the ET4000/W32i. The memory design method used on the schematic examples (See Appendix C) use four 256x16 DRAMs. In W32 designs, only 2 of these are installed for a total of 1MB DRAM. With the W32i, two or four DRAMs can be installed. The W32i has two additional signals, CASC* and CASD*, which available on pins 95 and 96, respectively, on the 160-pin W32i package.

Bit 0

Determines the width (from 16-bit to 32-bit) of the MD<31:0> bi-directional display memory data bus:

Bit 0	MD<31:24>	MD<23:16>	MD<15:8>	MD<7:0>	Bus Width
1	MD<31:24>	MD<23:16>	MD<15:8>	MD<7:0>	32
0		MD<15:8>	—	MD<7:0>	16

5.3.36 CRTC Indexed Register 3F: Horizontal Overflow

I/O address = 3#5

Bit	Description	Access
7	Row Offset Bit 8.	RW
6	Reserved.	
5	Reserved.	
4	Horizontal Sync Start Bit 8.	RW
3	Reserved.	
2	Horizontal Blank Start Bit 8.	RW
1	Reserved (always set to 0).	
0	Horizontal Total Bit 8.	RW

Bit **Description**

Bit 7 Provides a ninth bit to specify the amount to be added to the internal linear counter when advancing from one screen row to the next. See Section 5.3.22, CRTC Indexed Register 13: Row Offset.

Bit 4 Provides a ninth bit for the value of the internal horizontal character counter at which horizontal sync is to start. See Section 5.3.7, CRTC Indexed Register 4: Horizontal Sync Start.

Bit 2 Provides a ninth bit for the value of the internal horizontal character counter at which horizontal blanking is to start. See Section 5.3.6, CRTC Indexed Register 3: Horizontal Blank Start.

Bit 0 Provides a ninth bit to define the horizontal scan line time. See Section 5.3.3, CRTC Indexed Register 0: Horizontal Total.

5.4 TS Register Descriptions

The CPU interface to the ET4000/W32 internal Timing Sequencer (TS) consists of eight read/write registers. Of these registers, one register, the TS Index Register, is accessed by a separate independent I/O address (3C4). The remaining seven registers are internally indexed, which means that they are accessed via a common I/O address (3C5), with one of the seven registers that is actually selected by the TS Index register.

Table 5.4-1 TS Index Register

Register Name		Port Address
TS Index Register	(Read/Write)	3C4

Table 5.4-2 TS Indexed Registers

TS Indexed Register Name	TS Indexed Address		Port Address
Synchronous Reset	0	(Read/Write)	3C5
TS Mode	1	(Read/Write)	3C5
Write Plane Mask	2	(Read/Write)	3C5
Font Select	3	(Read/Write)	3C5
Memory Mode	4	(Read/Write)	3C5
Reserved	5		
TS State Control	6	(Read/Write)	3C5
TS Auxiliary Mode	7	(Read/Write)	3C5

5.4.1 TS Index

I/O address = 3C4

Bit	Description	Access
7:3	Reserved.	
2:0	Current TS index.	RW

Bit **Description**

Bits 2 0 Provide the index of the currently selected internally indexed register. The TS Index register determines which TS indexed register will be accessed when a read/write is performed using port address 3C5.

5.4.2 TS Indexed Registers

The following registers are TS indexed registers. These registers are accessed by first writing the index of the desired register to the TS Index register and then accessing the register using address 3C5.

5.4.3 TS Indexed Register 0: Synchronous Reset

I/O address = 3C5

Bit	Description	Access
7:2	Reserved.	
1	Synchronous reset control.	RW
0	Asynchronous reset control.	RW

Bit **Description**

Bit 1 When set to 0, commands the timing sequencer to synchronously clear and halt. Both bits 0 and 1 must be set to 1 for the timing sequencer to run.

For compatibility, a synchronous reset should be in effect whenever changing the Timing Sequencer or clock state. In general, synchronous reset periods should be kept as short as possible to prevent possible loss of display memory data.

Bit 0 When set to 0, commands the timing sequencer to synchronously clear and halt. When set to 1 the sequencer will run unless bit 1 is set to 0

5.4.4 TS Indexed Register 1: TS Mode

I/O address = 3C5

Bit	Description	Access
7:6	Reserved.	
5	Screen off (fast mode).	RW
4	Shift 4.	RW
3	Dot clocks/2.	RW
2	Video load/2.	RW
1	Reserved.	
0	Timing sequencer state (bit 0).	RW

Bit **Description**

Bit 5 When set to 1, will force blanking on the screen, allowing CPU access of video memory to go into a fast mode.

Bit 4 When set to 1, will allow the video shifter input latches to be loaded at quarter rate.

Bit 3 When set to 1, provides sequencer clocking at half the MCLK rate, known as dot clock/2 mode. This generates the dot clock signal at half the normal rate, effectively halving the pixel rate provided by the master clock. In VGA/EGA compatible operation, dot clock/2 mode is used in all display modes that have 320, rather than 640, pixels per scan line.

Bit 2 When set to 1, loads the video shifter (such as the ATC) input latches at half the video load rate.

Bit 0 This bit is used to set the timing sequencer state value. When set to a 0, the TS is set to State 0, or the 9 dot character clock; when set to a 1, the TS is set to State 1, or the 8-dot character clock.

5.4.5 TS Indexed Register 2: Write Plane Mask
I/O address = 3C5

Bit	Description	Access
7:4	Reserved.	
3	Write enable display memory plane 3.	RW
2	Write enable display memory plane 2.	RW
1	Write enable display memory plane 1.	RW
0	Write enable display memory plane 0.	RW

Bit	Description
Bits 3:0	The Write Plane Mask register enables or disables CPU write access to display memory planes on a plane-by-plane basis, and is only useful for 16-color (plane) systems. In 256 color mode, this register should be set to "0F" hex.

5.4.6 TS Indexed Register 3: Font Select
I/O address = 3C5

Bit	Description	Access
7:6	Reserved.	
5,3,2	Font Select B (FSB<2:0>).	RW
4,1,0	Font Select A (FSA<2:0>).	RW

Bit	Description
Bits 5:0	FSA or FSB (as selected by Attribute bit 3) is used to select one of eight possible soft fonts, providing two simultaneous character sets for display.

Based on the Selection bits derived, the font memories are selected as follows:

Selection Bits (SEL<2:0>)	Selected Segment	Offset in Font Memory
0 0 0	0	0
0 0 1	1	16K
0 1 0	2	32K
0 1 1	3	48K
1 0 0	4	8K
1 0 1	5	24K
1 1 0	6	40K
1 1 1	7	56K

NOTE: When ATC Indexed Register , bit 7> is set to 1, this register is not used. By using FS<2:0>, CC<7:0>, and RA<4:0> as listed in Tab7.3-13 4, 8 simultaneous fonts and character sets are available (B/W), and 4 and 4 respectively for Color. A total of 2048 character codes are available from which one could define 8 sets of 256 cc's each. 256 is a standard, albeit arbitrary number. the FS,CC, and RA pointers define which of the fonts and character sets are being used at a given time. If ATC Indexed Register 7, bit 7 is 0, this register is used as is.

5.4.7 TS Indexed Register 4: Memory Mode
I/O address = 3C5

Bit	Description	Access
7:4	Reserved.	
3	Enable Chain 4.	RW
2	Odd/even mode.	RW
1	Extended memory.	RW
0	Reserved.	

Bit	Description
Bit 3	When set to a 1, will enable Chain 4 (linear graphics) mode, where all four memories are chained linearly into a byte-oriented memory array whereby each byte will provide the eight bits (256-color) for each pixel. When set to 1, causes the two low-order bits of the address (A1 and A0) to select the plane that is accessed:

A<1:0>	Plane
0 0	0
0 1	1
1 0	2
1 1	3

When set to 0, the processor will access data sequentially in the bit plane

Bit 2	When set to 0, selects odd/even mode, in which even display memory planes (0 and 2) are active on display CPU accesses to even memory addresses (A0=0), while odd memory planes (1 and 3) are active on accesses to odd memory addresses (A0=1). When set to 1, causes the processor addresses to write to display memory planes according to the Write Map mask register.
Bit 1	When set to 1, enables selection among multiple fonts, where one of up to eight fonts can be selected (See Section 5.4.6, Font Select Register).

5.4.8 TS Indexed Register 6: TS State Control (protected by KEY)

I/O address = 3C5

Bit	Description	Access
7:3	Reserved.	
2:1	Timing sequencer state (bit 1 & 2).	RW
0	Reserved.	

Bit **Description**

Bits 2:1 These bits are used to set the extended timing sequencer state value. In conjunction with bit 0 of the TS Mode register, the additional states are used to define the number of dots per character in text mode:

TS Bit <2:1>	Mode 0	dots/char
1 1	1	16
1 0	0	12
0 1	1	11
0 1	0	10
0 0	1	8
0 0	0	9
1 0	1	7
1 1	0	6

IMPORTANT: All CRTC "character" timing calculations, with the exception of 9 dots/char are based on 8 dots/char regardless of the bit 1 and 2 of TS State Control Register's programmed value.

5.4.9 TS Indexed Register 7: TS Auxiliary Mode (protected by KEY)

I/O address = 3C5

Bit	Description	Access
7	VGA mode.	RW
6	Select MCLK/2 (if bit 0 is set to 0).RW	
5	BIOS ROM Address Map 2.	RW
4	Reserved (Set to 1 always).	RW
3	BIOS ROM Address Map 1.	RW
2	Reserved (Set to 1 always).	RW
1	Reserved.	
0	Select MCLK/4.	RW

Bit **Description**

Bit 7 When set to 1, enables VGA compatibility. A value of 0 will enable EGA compatibility. NOTE: The ET4000/W32 is set to default on power-up to VGA mode.

Bit 6 When set to 1, will divide the MCLK input clock frequency by two if bit 0 is equal to 0.

Bits 5,3 These bits are used for selection of ROM BIOS address space:

Bit 3 5	ROM BIOS Address Map Space Allocation	Total Memory Used
0 0	C0000-C3FFF	16KB
0 1	disabled	0KB
1 0	C0000-C5FFF; C6800-C7FFF	30KB
1 1	C0000-C7FFF*	32KB

* Power-up default

Bit 0 When set to 1, will divide the MCLK input clock frequency by 4.

5.5 GDC Register Descriptions

The CPU interface to the ET4000/W32 internal Graphics Data Controller (GDC) consists of 11 read/write registers. Of these registers, two are accessed by separate independent I/O addresses. The remaining 9 registers are internally indexed, which means that they are accessed via a common I/O address (3CF), with one of the 9 registers that is actually accessed selected by the GDC Index register.

Table 5.5-1 GDC Registers and Addresses

Register Name	Port Address	Indexed Address
Segment Select 1	R/W : 3CD	
Segment Select 2	R/W : 3CB	
GDC Index register	R/W : 3CE	
Indexed Register Name		
Set/Reset	R/W : 3CF	0
Enable Set/Reset	R/W : 3CF	1
Color Compare	R/W : 3CF	2
Data Rotate	R/W : 3CF	3
Read Plane Select	R/W : 3CF	4
GDC Mode	R/W : 3CF	5
Miscellaneous	R/W : 3CF	6
Color Care	R/W : 3CF	7
Bit Mask	R/W : 3CF	8

5.5.1 GDC Segment Select

I/O address = 3CB,3CD

Bit 3CB	Bit 3CD	Description	Access
5:4	7:4	Read segment pointer (RSP<5:0>).	RW
1:0	3:0	Write segment pointer (WSP<5:0>).	RW

Bit **Description**

When CRTC Indexed Register 36 (Video System Configuration 1) bit 4 is set to 0, then.

Bit
5:4 3CB — A 6-bit segment pointer selects one of 64 segments
7:4 3CD — (segment 0 to F) for CPU read operations.

Bits
1:0 3CB — A 6-bit segment pointer selects one of 64 segments
3:0 3CD — (segment 0 to F) for CPU write operations.

To enable the access of this register, the "KEY" must be set at least once after each power on reset or a synchronous reset (done by setting TS Indexed Register bit 1=0).

5.5.2 GDC Index

I/O address = 3CE

Bit	Description	Access
7:4	Reserved.	
3:0	Current index.	RW

Bit **Description**

Bits 3:0 — Provide the index of the currently selected internally indexed register. The GDC Index register determines which GDC indexed register will be accessed when a read/write is performed using port address 3CF.

5.5.3 GDC Indexed Registers

The remaining GDC registers are indexed registers, accessed by first writing the index value into the GDC Index register, and then accessing the indexed register using port address 3CF.

5.5.4 GDC Indexed Register 0: Set/Reset

I/O address = 3CF

Bit	Description	Access
7:4	Reserved.	
3	Set/reset value for map 3.	RW
2	Set/reset value for map 2.	RW
1	Set/reset value for map 1.	RW
0	Set/reset value for map 0.	RW

Bit **Description**

Bits 3:0 — Each set/reset bit specifies the value to be written to all bits of the addressed byte of the corresponding memory map (or plane), 0 through 3, when the set/reset function is enabled for that map. (See Section 5.5.5, GDC Indexed Register 1.)

5.5.5 GDC Indexed Register 1: Enable Set/Reset
I/O address = 3CF

Bit	Description	Access
7:4	Reserved.	
3	Enable set/reset value for map 3.	RW
2	Enable set/reset value for map 2.	RW
1	Enable set/reset value for map 1.	RW
0	Enable set/reset value for map 0.	RW

Bit Bits 3:0

Description

Each enable set/reset bit enables or disables the set/reset function for the corresponding memory map (or plane), 0-3. When any of bits 0-3 are set to 0, the set/reset function in the corresponding plane will be disabled. When set to 1, the set/reset function will be enabled. When enabled, the set/reset function stores either a 0 or FF value in the addressed byte of a given plane, depending on the set/reset value (see Section 5.5.4, GDC Indexed Register 0). When set/reset is enabled for a plane, the logical functions (see Section 5.5.7, GDC Indexed Register 3) operate on the set/reset value for each plane and the latched data for that plane; the bit mask (see Section 5.5.12, GDC Indexed Register 8) is also in effect. When the set/reset function is disabled, the addressed byte in a given plane is written as a combination of latched and CPU data, according to the write mode in effect and the bit mask, and the set/reset value has no effect. The set/reset function has no effect in write mode 1.

5.5.6 GDC Indexed Register 2: Color Compare
I/O address = 3CF

Bit	Description	Access
7:4	Reserved.	
3	Color compare value for plane 3 bits	RW
2	Color compare value for plane 2 bits.	RW
1	Color compare value for plane 1 bits.	RW
0	Color compare value for plane 0 bits.	RW

Bit Bits 3:0

Description

The Color Compare register is used in read mode 1 to determine which pixels from the display memory location, read by the CPU, match a specified color. The 4-bit color value in the color compare register is compared to the 4-bit color value of each of the eight pixels, spread across the four planes.

From this comparison, a bit value of 1 is returned in the data byte to the CPU, at the position corresponding to each pixel that matches the Color Compare register, and 0 is returned for each pixel that does not match the Color Compare register. In other words, an 8-bit value is returned to identify the comparison for all eight pixels.

NOTE: Both the Color Compare and Color Care registers are useful only in the "PLANE" (16 colors) systems. In the "LINEAR BYTE" (256 colors) systems, the color compare operation should be performed at the CPU level.

5.5.7 GDC Indexed Register 3: Data Rotate and Function Select
I/O address = 3CF

Bit	Description	Access
7:5	Reserved.	
4:3	Function select.	RW
2:0	Rotate count.	RW

Bit Bits 4:3

Description

Select the logical operation to be performed by the ALU on incoming CPU data and latched data. The logical operation is performed on only those bits that are enabled by the bit mask register; mask-disabled bits are written as the latched value (resulting from previous memory reads) only. For those bits that are mask enabled, one of four logical operations may be performed between CPU data and latched data by setting the function select as follows:

Bit 4	Bit 3	Logical operation
0	0	MOVE CPU data through unchanged.
0	1	AND CPU data with latched data.
1	0	OR CPU data with latched data.
1	1	XOR CPU data with latched data.

Note that write mode 1 may be used to write latched data unmodified; the same effect could be obtained by ANDing a CPU data byte of FF, ORing or XORing a CPU data byte of 0, or by setting the bit mask register to 0. The logical functions operate in write modes 0, 2 and 3 only; they are ignored in write mode 1.

Bits 2:0 — These bits set the number of bits (0-7) by which CPU data should be rotated to the right before it is sent to the ALU for bit masking and logical functions. Rotation is circular, with bit 0 feeding back to bit 7.

5.5.8 GDC Indexed Register 4: Read Plane Select
I/O address = 3CF

Bit	Description	Access
7:2	Reserved.	
1:0	Place select.	RW

Bit Bits 1:0

Description

Select the memory plane 0-3 from which the addressed byte is to be read and returned on the CPU data bus, in the "PLANE" (16 colors) configurations. Only one plane can be read at any one time.

5.5.9 GDC Indexed Register 5: GDC Mode

I/O address = 3CF

Bit	Description	Access
7	Reserved.	
6	Enable 256 color mode.	RW
5	Shift.	RW
4	Odd/even mode.	RW
3	Read mode.	RW
2	Reserved.	
1:0	Write mode.	RW

Bit **Description**

Bit 6 When set to 0, permits the loading of the ATC's shift registers to be controlled by bit 5. When set to one, the registers are loaded to support the 256-color mode.

Bit 5 When set to 1, enables the ATC's shift registers to shift for pixel formatting to support the 320x200 4-color CGA mode.

Bit 4 When set to 1, to selects odd/even addressing mode, in which even maps are accessed with even addresses and odd maps are accessed with odd addresses. The function of this bit is to determine from which display map data is to be routed to the CPU data bus on a CPU read in odd/even mode. If bit 4 is 1 and the Read Map Select register selects either of two maps in a given pair, then the even map is selected if address line 0 is 0, and the odd map is selected if address line 0 is 1. Bit 2 of CRTC Timing Sequencer Indexed Register 4 should be set to 0 to select odd/even mode, to generate all address control other than the read data selection in odd/even addressing mode. Odd/even addressing mode is useful for text modes.

Bit 3 Selects the read mode. When bit 3 is 0 (Read Mode 0), the data read from the map indicated by the read map select register (see Section 5.5.8, GDC Indexed Register 4) is returned on the CPU data bus. This is the normal read mode of operation. When bit 3 is 1, the color compare operation is enabled on a CPU read (See Section 5.5.6, Color Compare Register).

Bits 1:0 These bits select the mode in which data bytes are to be written to screen memory. The write modes are:

Bit (1:0)	Write Mode Selected
0 0	Write mode 0. Each CPU data byte written to display memory, as modified by the current rotation setting (see Section 5.5.7, GDC Indexed Register 3), is combined with the latched data for each map according to the current logical function (see Section 5.5.7, GDC Indexed Register 3) and written to each memory map. The byte written by the CPU is passed identically to the ALU for each map; differences in the byte actually written to the screen may occur due to differences in the latch contents for different maps. If the set/reset function is enabled for any map (see Section 5.5.5, GDC Indexed Register 1), then the set/reset bit value for that map (see Section 5.5.4, GDC Indexed Register 0) is written to every bit of the addressed byte of that map regardless of the CPU data. The bit mask (see Section 5.5.12, GDC Indexed Register 8) applies in write mode 0, and causes the latch data alone to be written to each bit that is mask disabled.
0 1	Write mode 1. The data contained in the latches is written unmodified to the addressed byte in screen memory. All maps are written. This is useful for rapid data movement from display memory to display memory, as all maps can be latched with a single read and then written with a single write mode 1 operation. The bit mask is ignored, as is the selected logical function. The set/reset function is also ignored
1 0	Write mode 2. Each bit, 0-3, of the data written by the CPU is extended to a byte and written to the four corresponding planes. Bit 0 of the data byte is extended to a byte and written to the addressed byte of map 0, bit 1 is extended to a byte and written to map 1, and so on up to bit 3, which is extended to a byte and written to map 3. The bit mask applies to the data byte for each map; that is, after the bit for each map from the CPU data written is extended to a byte, the byte for each map is masked as if it were the CPU data byte. The selected logical function operates normally on the byte for each map and the latched data for that map. The set/reset operation functions normally, overriding the write mode 2 bit for a given map when enabled. The data rotate register has no effect in write mode 2.
1 1	Write mode 3. Eight bits of the value contained in the Set/Reset register are written for each map. Rotated CPU data are ANDed with data from the bit mask register (see Section 5.5.12, GDC Indexed Register 8) to produce an 8-bit value that functions as the bit mask register does in write modes 0 and 2.

5.5.10 GDC Indexed Register 6: Miscellaneous

I/O address = 3CF

Bit	Description	Access
7:4	Reserved (= 0).	
3:2	Memory map.	RW
1	Enable odd/even mode.	RW
0	Graphics mode enable.	RW

Bit **Description**

Bits 3:2 Memory Map—Control mapping of the Frame Buffer into CPU address space. NOTE: Bits 2&3 should be set to 0 when bit 4 of CRTC Indexed Register 36 is set to 1 (linear system).

See Section 7.3 for the effect this bit has on the Video Memory Map.

Bit 1 When set to 1, enables odd/even mode. will cause the replacement of the CPU address bit 0 with a high-order bit, and the odd/even maps are "chained" via the CPU A0 bit.

Bit 0 When set to 1, enables graphics mode.

5.5.11 GDC Indexed Register 7: Color Care
I/O address = 3CF

Bit	Description	Access
7:4	Reserved.	
3	Enable color compare color output 3.	RW
2	Enable color compare color output 2.	RW
1	Enable color compare color output 1.	RW
0	Enable color compare color output 0.	RW

Bit	Description
Bits 3:0	Each bit enables or disables the participation of the corresponding plane in a read mode 1 color comparison. If a bit is 1, then the color compare is enabled for that plane (see Section 5.5.6, GDC Indexed Register 2: Color Compare). If a bit is 0, then the value in that plane has no effect on the value returned by the color comparison.

5.5.12 GDC Indexed Register 8: Bit Mask
I/O address = 3CF

Bit	Description	Access
7:0	Controls CPU data routing for corresponding bits of addressed screen map byte.	RW

Bit	Description
Bits 7:0	Each bit of the Bit Mask register either blocks the corresponding CPU data bit from affecting the value written to the screen or allows the CPU data bit through. A zero (0) value blocks and a 1 value passes CPU data. If a given bit is blocked, the value stored in that bit of each data latch (one for each plane) is sent to the corresponding screen plane. If a given bit is enabled, the value in that bit position of the CPU data is passed to the ALU, where it can be mixed with latched data via the selected logical function. The data will be rotated (see Section 5.5.7, GDC Indexed Register 3) before it is masked.

5.6 ATC Register Descriptions

The CPU interface to the ET4000/W32 internal Attribute Controller (ATC) consists of 23 read/write registers, and a separate flip-flop (1-bit register) which can be toggled between index/data mode. Two I/O addresses are used in conjunction with the index/data mode flip-flop to access the 23 registers as follows: An I/O read to the Input Status 1 register (3BA or 3DA depending on monochrome or color mode respectively, as controlled by bit 0 in the Miscellaneous Output Register) will reset the index/data flip-flop to index mode. Every I/O write with port address 3C0 will also toggle the index/data flip-flop between index and data mode. The index value in the ATC index register can be read with I/O address 3C0. While in index mode, the index value can be written to the ATC index register with I/O address 3C0, with the index/data mode flip-flop toggled to the data mode.

If the 16-bit I/O is enabled, an I/O WORD access to port 3C0 will automatically reset the index/data flip-flop. All of the 23 indexed registers can be read with I/O address 3C1. While in data mode, all of these indexed registers can be written to with I/O address 3C0, with the index/data mode flip-flop toggled to the index mode.

Table 5.6-1 ATC Index Register

Register Name	Port Address	Indexed Address
ATC Index register	R : 3C0 W : 3C0 (INDEX)	

Table 5.6-2 ATC Indexed Registers

Indexed Register Name		
Palette	R : 3C1 W : 3C0 (DATA)	0-F
ATC Mode	R : 3C1 W : 3C0 (DATA)	10
Overscan	R : 3C1 W : 3C0 (DATA)	11
Color Plane Enable	R : 3C1 W : 3C0 (DATA)	12
Horizontal Pixel Panning	R : 3C1 W : 3C0 (DATA)	13
Color Reset	R : 3C1 W : 3C0 (DATA)	14
Miscellaneous	R : 3C1 W : 3C0 (DATA)	16
Miscellaneous	R : 3C1 W : 3C0 (DATA)	17

5.6.1 ATC Index

R : Port address = 3C0
W : Port address = 3C0 (index/data flip-flop in INDEX mode)

Bit	Description	Access
7:6	Reserved.	
5	Palette RAM address source.	RW
4:0	Current ATC index.	RW

Bit	Description
Bit 5	A value of 0 enables CPU write access to palette RAM, and replaces all video outputs with the contents of the overscan register. A value of 1 disables CPU write access to palette RAM and allows ATC access of RAM. This bit must be set to 0 before the CPU can update any palette RAM location. After the palette RAM is updated, this bit must be set to 1 so the ATC can access the palette RAM for video information.

Bits 4:0 Provide the index of the currently selected internally indexed register.

5.6.2 ATC Indexed Registers

The following registers are the ATC indexed registers. These registers are accessed by writing the index of the desired register to the ATC Index register when the index/data flip-flop is in INDEX mode, and then accessed using the index value in the ATC Index Register. See details under previous paragraphs under ATC Register Descriptions.

5.6.3 ATC Indexed Registers 0-F: Palette RAM

R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description	Access
7	Reserved.	
6	Reserved.	
5	Secondary red video.	RW
4	Secondary green/intensity video.	RW
3	Secondary blue/mono video.	RW
2	Primary red video.	RW
1	Primary green video.	RW
0	Primary blue video.	RW

These 16 internal palette registers define a dynamic remapping between colors as defined by text attributes and graphics bit maps and the colors actually generated by the video circuitry. Each palette register 0-15 corresponds to an attribute, 0-15, in the "PLANE" (16 colors) configuration. Four bits (1 bit from each plane) of video data for a given pixel enters the palette RAM and addresses one of the 16 palette registers, and the 6-bit value stored in the corresponding palette register is transferred to the output latch of the ATC to provide the actual pixel data. In "linear byte" (256 colors) configuration, these registers should be programmed to have contents the same as the indexed address to "pass through" the internal display data.

Bit	Description
Bits 5:0	When set to 1, select the appropriate color attribute. When set to 0, indicate the appropriate color is not present.

5.6.4 ATC Indexed Register 10: Mode Control

R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description	Access
7	SB/SG select.	RW
6	PELCLOCK/2.	RW
5	Enable pixel panning.	RW
4	Reserved.	
3	Background intensity/blink.	RW
2	Line graphics enable.	RW
1	Mono/color select.	RW
0	Graphics/text select.	RW

Bit **Description**

Bit 7 Used to select for the SB and SG video bits. When set to 1, SB and SG are bits 0 and 1, respectively, of the Color Select Register; a zero (0) causes them to be bits 4 and 5 of the internal palette register. This is not applicable to linear graphics (256-color) modes, for which SB and SG always come from memory data.

Bit 6 When set to 1, halves the rate of pixel output to the screen such that only 4, as opposed to the usual 8, pixels are output in a character clock time. This is normally used only for the 320x200 256-color graphics mode. For all other 256-color modes, this bit should be set to 0.

Bit 5 When set to one (1), disables pixel panning while in split screen, while a 0 will enable the panning.

Bit 3 When set to 1, enables blinking in both text and graphics modes. When enabled in text mode, blinking occurs whenever bit 7 of the attribute byte for a given character is 1; when enabled in graphics mode, blinking occurs for all bits that have a 1 in the intensity plane. Blinking is performed by toggling the most significant address line (bit 3) into the palette RAM, thus toggling the video data between the lower eight and upper eight palette RAM registers. This means that the effect of the blink (for example, reverse video to video, video to high-intensity video, dark to dark) is completely programmable. Bit-mapped graphics modes can be programmed to support all the attributes of text modes, for instance.

NOTE: The non-blinking bits will use the upper eight palette registers.

When set to 0, disables blinking; in this case bit 3 of the palette RAM address is multiplexed directly from the video data to the palette RAM. When bit 3 is 0, all 16 simultaneous colors are enabled in graphics mode; in text mode, all 16 background colors are available simultaneously.

Bit 2 When set to 1, specifies that in the 9 dots/character state (controlled by the CRTC), the ninth (and last) dot produced horizontally per character should replicate the eighth dot for character codes C0 hex through DF hex. The ninth dot of all other character codes is always 0 when line graphics is enabled. This is normally used to allow the text mode line graphics characters supported on the IBM Monochrome Display, which are 8-dot-wide characters in a 9-dot-wide character box, to connect. If this bit is 0 and the CRTC is set to the 9 dots/character state, then the 9th dot will display bit 7 of Intensity Memory plane (plane 3).

Bit 1 When set to 1, selects a monochrome display attribute; when set to 0, enables a color display attribute.

Bit 0 When set to 1, enables the ATC to process the pixel data in graphics mode; when set to 0, enables the ATC to process the pixel data in text mode.

5.6.5 ATC Indexed Register 11: Overscan Color

R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description	Access
7	Secondary Intensity border color.	RW
6	Secondary Red border color.	RW
5	Secondary Green border color.	RW
4	Secondary Blue border color.	RW
3	Intensity border color.	RW
2	Red border color.	RW
1	Green border color.	RW
0	Blue border color.	RW

This register defines the color to be displayed around the perimeter of the working screen area (the border or overscan color).

Bit **Description**

Bits 7:0 When set to 1, select the appropriate border color/attribute, each bit corresponding to one of the output pins. This value is a 0 for the monochrome display.

5.6.6 ATC Indexed Register 12: Color Plane Enable

R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description	Access
7:6	Reserved.	
5:4	Video status select.	RW
3:0	Enable plane.	RW

Bit **Description**

Bits 5:4 These bits select two of eight color outputs to be returned by the Status register, as follows:

Input Status Register 1

Bit		Bit	
5	4	5	4
0	0	PR	PB
0	1	SG	SB
1	0	PI	PG
1	1	SI	SR

Bits 3:0 In "PLANE" (16 colors) configuration, the color plane relative to each of bits 0-3 is enabled when the appropriate individual bits are set to one. Bits 0,1,2,3 control the enabling of planes 0,1,2,3, respectively.

5.6.7 ATC Indexed Register 13: Horizontal Pixel Panning

R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description	Access
7:4	Reserved.	
3:0	Horizontal pixel panning.	RW

Bit	Description
Bits 3:0	These bits specify the number of pixels by which the video data should be shifted to the left. Shifts of up to nine pixels are supported. Note that in 9-dot modes, a value of 8 signifies no shift, and the values of 0-7 signify shifts of 1-8 pixels, respectively. NOTE: In 6- and 7-dot modes, values of 2 and 1, respectively, signify no shift.

5.6.8 ATC Indexed Register 14: Color Select

R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description	Access
7:4	Reserved.	
3	S_color 7.	RW
2	S_color 6.	RW
1	S_color 5.	RW
0	S_color 4.	RW

Bit	Description
Bits 3:2	Provide the two high-order bits of the exported digital color value in plane systems. With 256-color graphic modes, the 8-bit attribute value becomes the 8-bit digital value exported from the chip.
Bits 1:0	Available for replacement use of bits 5 and 4 of the attribute palette registers, forming an 8-bit value for color to be exported from the chip. When bit 7 of the ATC Mode register is set to 1, bits 1 and 0 are selected as SG and SB outputs of the plane system.

5.6.9 ATC Indexed Register 16: Miscellaneous (protected by KEY)

R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description	Access
7	Bypass the internal palette.	RW
6	2-byte character code enable.	RW
5:4	Select High Resolution/color mode.	RW
3:2	Reserved.	
1	Protect external DAC.	RW
0	Protect border.	RW

Bit	Description
Bit 7	When set to 1, causes the internal palette to be bypassed (effectively, the output value equals the input value).
Bit 6	When set to 1, enables the ATSK bit (attribute skew). This is used to enable a 2-byte Character Code (CC) feature. The ATSK bit will be used to compensate the attribute (ATT), Display Enable (DE) and Cursor Skew. Therefore, no external hardware circuit is needed for ATT, DE, and Cursor skew compensation. * For the first font fetch (i.e.: RASBL and CASL<3:2> DRAM access cycle) of each scan line, the MD<31:16> font data are ignored. * The first or subsequent Character Codes (CC0 or CC1, CC2, etc.) should be latched by the external circuit and this Character Code should remain latched until the next font fetch cycle. * The second, or odd, Character Code (CC1 or CC3, CC5, etc.) and the previously latched even Character Code (CC0 or CC2, CC4, etc.) total of 16-bit Character Codes should be latched at the beginning of every even font fetch cycle via transparent latches. * If the current CCn is not an English character, then the font data (MD<31:16>) will be fetched according to the 16-bit Character Code (i.e., the external EPROMs are enabled), else the DRAMs font (which contains the VGA's font) are enabled. * If the last character font of the scan line is a 24-bit wide font and begins at an odd column, then only half of the font (12-dot) will be displayed.
Bits 5:4	These bits, in combination, select normal power-up 8-bit per PCLK or else 16-bit per PCLK (AP<15:0> output. Note that to support ET4000 Rev. G's high color mode, configure CRTC and ATC to 8 bit per pixel (256 color mode) and clock AP<7:0> with double-clocking. Bit 5 4 0 0 Normal power-up default (8-bit/clock) 1 0 16 bit per clock mode 0 1 Reserved 1 1 Reserved
Bit 1	When set to 1, disables I/O writes to External/Internal Palette RAM. Normal power-up default is set to 0.
Bit 0	When set to 1, disables I/O writes to Overscan Color register bits <3:0>. Normal power-up default is set to 0.

5.6.10 ATC Indexed Register 17: Miscellaneous 1 (protected by KEY)

R : Port address = 3C1
W : Port address = 3C0 (index/data flip-flop in DATA mode)

Bit	Description	Access
7	Redefine attribute (SMAE).	RW
6:0	Reserved.	

Bit **Description**

Bit 7 When set to 1, protects the internal palette RAM and is used to redefine the attribute bits as follows:

Monochrome

Attribute

Bit	Description
7	Normal/reverse video
6	Full/half intensity
5	Character visible/invisible
4	Underline off/on
3	Blinking off/on
2:0	Font select

Bit 7 When set to 1, enables the reverse video attribute. When set to 0, displays normal video

Bit 6 When set to 1, changes the character intensity to half. When set to 0, displays full intensity.

Bit 5 When set to 1, disables characters from being displayed. When set to 0, enables normal character display.

Bit 4 When set to 1, turns the underline attribute on. When set to 0, enables normal character display

Bit 3 When set to 1, turns the blinking attribute on. When set to 0, enables normal character display.

Bits 2:0 Used to select up to eight simultaneous soft fonts and up eight simultaneous character sets for display. See Table 5.3-4 CPU/CRTC Addressing Modes, note 4; bits <2:0> here correspond to FS<1:0,2> in the table. (When ATC Indexed Register 17 bit 7 is set to 1 TS Indexed Register 3: Font Select is not used.)

Note that to get the attributes indicated here the ATC Palette RAM registers 0-7 must be programmed to 0,0,0,0,18,0,8,0 where 0=off, 8=half intensity, and 18=full intensity, and blinking should be enabled (via ATC Indexed Register 10 bit 3).

Color

Attribute

bit	Description
7	Background red
6	Background green
5	Background blue
4	Foreground red
3	Foreground green
2	Foreground blue
1-0	Font select

Bits 7:5 When set to 1, are used to select background colors of red, green, and blue, respectively.

Bits 4:2 When set to 1, are used to select foreground colors of red, green, and blue, respectively.

Bits 1:0 Used to select up to four simultaneous soft fonts and up to four simultaneous character sets for display. Bit 2 is not used for font select for color operation. See Table 5.3-4 CPU/CRTC Addressing Modes, note 4. (When ATC I<7> is set to 1 TS Indexed Register 3: Font Select is not used.)

Note that to get the attributes indicated here, the ATC Palette RAM registers 8-F should be set equal to register 0-7 (registers 0-7 containing the normal range of colors), and blinking should be disabled (via ATC Indexed Register 10 bit 3). Also, the underline register (CRTC Indexed Register 14) should be set >= the character height.

5.7 CRTCB/Sprite Register Descriptions

Index	Register
E0	CRTCB/Sprite Horizontal Pixel Position Low
E1	CRTCB/Sprite Horizontal Pixel Position High
E2	CRTCB Width Low/Sprite Horizontal Preset
E3	CRTCB Width High
E4	CRTCB/Sprite Vertical Pixel Position Low
E5	CRTCB/Sprite Vertical Pixel Position High
E6	CRTCB Height Low/Sprite Vertical Preset
E7	CRTCB Height High
E8	CRTCB/Sprite Starting Address Low
E9	CRTCB/Sprite Starting Address Middle
EA	CRTCB/Sprite Starting Address High
EB	CRTCB/Sprite Row Offset Low
EC	CRTCB/Sprite Row Offset High
ED	CRTCB Pixel Panning
EE	CRTCB Color Depth
EF	CRTCB/Sprite Control

The CRTCB/Sprite registers are accessed using an indexed addressing scheme whereby a number selecting a register is first written to address 21xA (Index) and then the register can be read from or written to at address 21xB. The CRTCB/Sprite registers use indices E0 through EF.

The Index Register at address 21xA is also used to address the IMA Indexed Registers, see Section 5.8 for details.

The value of 'x' in the addresses 21xA and 21xB is determined by the logical value on the IOD<2:0> pins of the chip at power-up reset; see Section 3 for details.

5.7.1 CRTCB Index Register

I/O address = 21xA

Bit	Description	Access
7:0	Indexed register select.	RW

Bit	Description
Bits 7:0	This register is used to select the CRTCB/Sprite indexed register that is accessed when address 21xB is read or written.

5.7.2 CRTCB/Sprite Horizontal Pixel Position Low (Index: E0)

I/O address = 21xB

Bit	Description	Access
7:0	Horizontal pixel position, bits <7:0>.	RW

5.7.3 CRTCB/Sprite Horizontal Pixel Position High (Index: E1)

I/O address = 21xB

Bit	Description	Access
7:4	Reserved.	
3:0	Horizontal pixel position, bits <11:8>.	RW

Bit	Description
Bits 11:0	The Horizontal Pixel Position is the position in pixels of the leftmost edge of the actively displayed portion of the CRTCB window or Sprite, relative to the leftmost edge of the CRTC active picture area.

5.7.4 CRTCB Width Low/Sprite Horizontal Preset (Index: E2)

I/O address = 21xB

Bit	Description	Access
7:0	CRTCB width, bits <7:0>/Sprite horizontal preset.	RW

Bit	Description
Bits 7:0	When the CRTCB is selected (with CRTCB/Sprite Indexed Register EF, bit 0), this register contains bits <7:0> of the 12-bit value defining the width of the CRTCB window in pixels. The value loaded should be 1 less than the desired width. When the Sprite is selected, bits <5:0> specify the Horizontal Pixel Preset. That is, the horizontal position relative to the beginning of the sprite area at which display of the sprite starts. The sprite does not wrap and always ends at position 63. See also Section 2.2 Secondary CRTC/Sprite (CRTCB).

NOTE: Programming of the CRTCB display area must not exceed the boundaries of the CRTC (primary) display area. This restriction does not apply when the Sprite is enabled.

5.7.5 CRTCB Width High (Index: E3)
I/O address = 21xB

Bit	Description	Access
7:4	Reserved.	
3:0	CRTCB width, bits <11:8>.	RW

Bit	Description
Bits 3:0	When the CRTCB is selected (with CRTCB/Sprite Indexed Register EF, bit 0), this register contains bits <11:8> of the 12-bit value defining the width of the CRTCB window in pixels. The value loaded should be 1 less than the desired width.

NOTE: Programming of the CRTCB display area must not exceed the boundaries of the CRTC (primary) display area. This restriction does not apply when the Sprite is enabled.

5.7.6 CRTCB/Sprite Vertical Pixel Position Low (Index: E4)
I/O address = 21xB

Bit	Description	Access
7:0	Vertical pixel position, bits <7:0>.	RW

5.7.7 CRTCB/Sprite Vertical Pixel Position High (Index: E5)
I/O address = 21xB

Bit	Description	Access
7:4	Reserved	
3:0	Vertical pixel position, bits <11:8>.	RW

Bit	Description
Bits 11:0	The Vertical Pixel Position is the position in scan lines of the topmost edge of the actively displayed portion of the CRTCB window or Sprite, relative to the topmost edge of CRTC active picture area.

5.7.8 CRTCB Height Low/Sprite Vertical Preset (Index: E6)
I/O address = 21xB

Bit	Description	Access
7:0	CRTCB height, bits<7:0>/Sprite Vertical Preset.	RW

Bit	Description
Bits 7:0	When the CRTCB is selected (with CRTCB/Sprite Indexed Register EF, bit 0), this register contains bits <7:0> of the 12-bit value defining the height of the CRTCB window in scan lines. The value loaded should be 1 less than the desired height. When the Sprite is selected, bits <5:0> specify the Vertical Pixel Preset. That is, the vertical position relative to the beginning of the 64x64 pixel sprite area at which display of the sprite starts. The sprite does not wrap and always ends at position 63. See also Section 2.2 Secondary CRTC/Sprite (CRTCB).

NOTE: Programming of the CRTCB display area must not exceed the boundaries of the CRTC (primary) display area. This restriction does not apply when the Sprite is enabled.

5.7.9 CRTCB Height High (Index: E7)
I/O address = 21xB

Bit	Description	Access
7:4	Reserved.	
3:0	CRTCB height, bits <11:8>.	RW

Bit	Description
Bits 3:0	When the CRTCB is selected (with CRTCB/Sprite Indexed Register EF, bit 0), this register contains bits <11:8> of the 12-bit value defining the height of the CRTCB window in scan lines. The value loaded should be 1 less than the desired height.

NOTE: Programming of the CRTCB display area must not exceed the boundaries of the CRTC (primary) display area. This restriction does not apply when the Sprite is enabled.

5.7.10 CRTCB/Sprite Starting Address Low Register (Index: E8)
I/O address = 21xB

Bit	Description	Access
7:0	CRTCB/Sprite starting address, bits <7:0>.	RW

5.7.11 CRTCB/Sprite Starting Address Middle Register (Index: E9)
I/O address = 21xB

Bit	Description	Access
7:0	CRTCB/Sprite starting address, bits <15:8>.	RW

5.7.12 CRTCB/Sprite Starting Address High Register (Index: EA)
I/O address = 21xB

Bit	Description	Access
7:4	Reserved.	
3:0	CRTCB/Sprite starting address, bits <19:16>.	RW

Bit	Description
Bits 19:0	These three registers define a 20-bit offset into display memory at which the CRTCB/Sprite pixel data is located. The starting address is measured in double words, so if the data resides at byte address 256, then a value of 64 (i.e., 256/4) should be programmed into these registers.

5.7.13 CRTCB/Sprite Row Offset Low Register (Index: EB)
I/O address = 21xB

Bit	Description	Access
7:0	Memory address offset, bits <7:0>.	RW

5.7.14 CRTCB/Sprite Row Offset High Register (Index: EC)
I/O address = 21xB

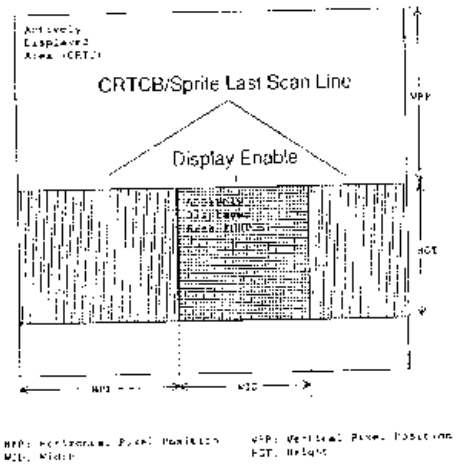
Bit	Description	Access
7:4	Reserved.	
3:0	Memory address offset, bits <11:8>.	RW

Bit	Description
Bits 11:0	These two registers specify the number of quadwords between the start of one row of the CRTCB pixel map to the start of the next row. This field MUST be programmed to "2" when the Sprite is enabled.

5.7.15 CRTCB Pixel Panning (Index: ED)
I/O address = 21xB

Bit	Description	Access
7	CRTCB/Sprite last scan line.	RO
6	Display enable.	RO
5:3	Reserved.	
2:0	CRTCB pixel panning.	RW

Bit	Description
Bit 7	When high indicates the last scan line has been displayed for the CRTCB/Sprite.
Bit 6	This bit reflects real time status of the BDE pin (See Section 3.7.2) for CRTCB/Sprite.
Bits 2:0	This value specifies the number of pixels by which the video data should be shifted to the left. Shifts of up to nine pixels are supported. Note that in 9-dot modes, a value of 8 signifies no shift, and the values of 0-7 signify shifts of 1-8 pixels, respectively.



CRTCB Window Positioning

5.7.16 CRTCB Color Depth Register (Index: EE)

I/O address = 21xB

Bit	Description	Access
7:6	Vertical zoom factor	RW
5:4	Reserved..	
3:0	CRTCB bits/pixel select.	RW

Bit	Description
Bits 7:6	The value of these two bits determine the number of times the line is repeated.

Bit 7:6	times line repeated (no. of times each line is relicated)
0 0	1
0 1	2
1 0	3
1 1	4

Bits 3:0 This value selects the color depth for the CRTCB. Combinations for color depth beyond 16 bits/pixel are currently reserved.

Bit 3 2 1 0	Bit/pixel
0 0 0 0	1
0 0 0 1	2
0 0 1 0	4
0 0 1 1	8
0 1 0 0	16
. . . .	
1 1 1 1	Reserved.

5.7.17 CRTCB/Sprite Control (Index: EF)

I/O address = 21xB

Bit	Description	Access
7:2	Reserved.	
2	Sprite size control.	RW
1	B pixel overlay/B pixel data output.	RW
0	CRTCB/Sprite select.	RW

Bit	Description
Bit 2	When set to 1, sets sprite size to 128x128. When set to 0, specifies sprite size at 64x64.
Bit 1	When set to 1, specifies that the CRTCB pixels overlay the CRTC (i.e., normally displayed) pixels. When set to 0, the CRTCB pixel data (2-bit sprite) is output to the SP<1:0> pins.
Bit 0	When set to 1, selects the CRTCB functioning. When set to 0, selects the sprite. See also Section 5.8.9, IMA Indexed Register F7.

5.8 IMA Register Descriptions

IMA Indexed Registers

Index	Register
F0	Image Starting Address Low
F1	Image Starting Address Middle
F2	Image Starting Address High
F3	Image Transfer Length Low
F4	Image Transfer Length High
F5	Image Row Offset Low
F6	Image Row Offset High
F7	Image Port Control

5.8.1 Indexed Addressing

The IMA registers are accessed using an indexed addressing scheme whereby a number selecting a register is first written to address 21xA (Index) and then the register can be read from or written to at address 21xB. The IMA registers use indices F0 through F7.

The Index Register at address 21xA is also used to address the CRTC/Sprite Indexed Registers, see Section 5.7 for details.

The value of 'x' in the addresses 21xA and 21xB is determined by the logical value on the IOD<2:0> pins of the chip at power-up reset; see Section 3 for details.

5.8.2 IMA Indexed Register F0: Image Starting Address Low

I/O address = 21xB

Bit	Description	Access
7:0	Image starting address, bits <7:0>.	RW

5.8.3 IMA Indexed Register F1: Image Starting Address Middle

I/O address = 21xB

Bit	Description	Access
7:0	Image starting address, bits <15:8>.	RW

5.8.4 IMA Indexed Register F2: Image Starting Address High

I/O address = 21xB

Bit	Description	Access
7:4	Reserved.	
3:0	Image starting address, bits <19:16>.	RW

Bit	Description
Bits 19:0	These three registers define a 20-bit offset into display memory at which the image data is to be stored. The starting address is measured in double words, so if the data is to be stored at byte address 256, then a value of 64 (i.e., 256/4) should be programmed into these registers.

5.8.5 IMA Indexed Register F3: Image Transfer Length Low
I/O address = 21xB

Bit	Description	Access
7:0	Image width, bits <7:0>.	RW

5.8.6 IMA Indexed Register F4: Image Transfer Length High
I/O address = 21xB

Bit	Description	Access
7:4	Reserved.	
3:0	Image width, bits <11:8>.	RW

Bit	Description
Bits 11:0	These two registers define a 12-bit value which is the number of doublewords to be transferred per scan line.

5.8.7 IMA Indexed Register F5: Image Row Offset Low
I/O address = 21xB

Bit	Description	Access
7:0	Memory address offset, bits <7:0>.	RW

5.8.8 IMA Indexed Register F6: Image Row Offset High
I/O address = 21xB

Bit	Description	Access
7:4	Reserved.	
3:0	Memory address offset, bits <11:8>.	RW

Bit	Description
Bits 11:0	These two registers specify the number of doublewords between the start of one row of the stored image data and the start of the next row.

5.8.9 IMA Indexed Register F7: Image Port Control
I/O Address = 21xB

Bit	Description	Access
7	CRTCB/Sprite enable.	RW
6:2	Reserved.	
1	Interlace Image Port address.	RW
0	Image Port enable.	RW

Bit	Description
Bit 7	When set to 1, enables the CRTCB or the Sprite, whichever is selected in CRTCB/Sprite Indexed Register EF, bit 0. When set to 0, disables CRTCB or Sprite. At reset, this bit has a value of 0.
Bit 1	When set to 1, enables odd/even interlace transfer. When set to 0, enables linear interlace transfer. See Section 2.2.7 for additional information. At reset, this bit has a value of 0.
Bit 0	When set to 1, enables the Image Port. (See Section 3.8 Image Port Interface for shared pin information.) When set to 0, disables the Image Port, meaning that all the inputs to the Image Port are ignored and the pins assume their alternate functions. At reset, this bit has a value of 0.

5.9 MMU Register Descriptions

See Section 7.3 for the memory base address for the MMU registers. The offset in the table below is added to the base address to calculate the actual address of the register.

Memory Offset	Register
00	MMU Memory Base Pointer Register 0
04	MMU Memory Base Pointer Register 1
08	MMU Memory Base Pointer Register 2
13	MMU Control Register

5.9.1 MMU Memory Base Pointer Register 0

Memory offset = 00

Bit	Description	Access
31:22	Reserved.	
21:0	Memory base pointer.	RW

Bit	Description
Bits 21:0	The base pointer defines the starting address in display memory of MMU aperture number 0.

5.9.2 MMU Memory Base Pointer Register 1

Memory offset = 04

Bit	Description	Access
31:22	Reserved.	
21:0	Memory base pointer.	RW

Bit	Description
Bits 21:0	The base pointer defines the starting address in display memory of MMU aperture number 1.

5.9.3 MMU Memory Base Pointer Register 2

Memory offset = 08

Bit	Description	Access
31:22	Reserved.	
21:0	Memory base pointer.	RW

Bit	Description
Bits 21:0	The base pointer defines the starting address in display memory of MMU aperture number 2.

5.9.4 MMU Control Register

Memory offset = 13

Bit	Description	Access
7	Reserved.	
6:4	Linear Address Control (LAC).	RW
3	Reserved.	
2:0	Aperture type (APT)	RW

Bit	Description
Bits 6:4	There is one Linear Address Control bit for each MMU aperture. Bit 6 of this register corresponds to MMU aperture 2, bit 5 to aperture 1, and bit 4 to aperture 0. When set to 0, the memory is organized according to the current display mode. When set to 1, the memory is organized in linear fashion. The effect is as if the following register modifications were made: TS2<3:0>=1111 TS4<3>=1 GDC1<3:0>=0000 GDC3<4:0>=00000 GDC5<3>=0 GDC5<1:0>=00 GDC6<1>=0 GDC8<7:0>=11111111
Bits 2:0	There is one Aperture Type bit for each MMU aperture. Bit 2 of this register corresponds to MMU aperture 2, bit 1 to aperture 1, and bit 0 to aperture 0. This bit indicates whether an aperture is in "accelerated mode" or not. When set to 0, access through this MMU aperture is routed through the GDC to display memory. When set to 1, access through this MMU aperture is routed to the accelerator.

5.10 ACL Register Descriptions

See Section 7.3 for the memory base address for the MMU registers. The offset in the table below is added to the base address to calculate the actual address of the register.

Memory Offset	Register
	Non-Queued Registers
30	ACL Suspend/Terminate Register
31	ACL Operation State Register
32	ACL Sync Enable Register
34	ACL Interrupt Mask Register
35	ACL Interrupt Status Register
36	ACL Accelerator Status Register
	Queued Registers
80	ACL Pattern Address Register
84	ACL Source Address Register
88	ACL Pattern Y Offset Register
8A	ACL Source Y Offset Register
8C	ACL Destination Y Offset Register
8E	ACL Virtual Bus Size Register
8F	ACL X/Y Direction Register
90	ACL Pattern Wrap Register
92	ACL Source Wrap Register
94	ACL X Position Register
96	ACL Y Position Register
98	ACL X Count Register
9A	ACL Y Count Register
9C	ACL Routing Control Register
9D	ACL Reload Control Register
9E	ACL Background Raster Operation Register
9F	ACL Foreground Raster Operation Register
A0	ACL Destination Address Register

5.10.1 ACL Suspend/Terminate Register

This is a non-queued register
Memory offset = 30

Bit	Description	Access
7:4	Reserved.	
4	Terminate Accelerator Operation (TO).	RW
3:1	Reserved.	
0	Suspend Accelerator Operation (SO).	RW

Bit **Description**

Bit 4 Used to terminate an Accelerator operation. To terminate an Accelerator operation, the programmer should write a 1 to this bit, wait for RDST (ACL Status Register, bit 0) to be 0, then write a 0 to this bit.

Termination returns the accelerator to its initial power-on state, with the ACL registers returned to the values that they contain after a reset of the chip. The programmer is advised to treat all accelerator registers as having undefined values after a termination, and reprogram all registers before initiating another accelerator operation.

Bit 0 Used to suspend an Accelerator operation. To suspend an Accelerator operation, the programmer should write a 1 to this bit, wait for RDST (ACL Status Register, bit 0) to be 0, then write a 0 to this bit.

5.10.2 ACL Operation State Register

This is a non-queued register
Memory offset = 31

Bit	Description	Access
7:4	Reserved.	
3	Resume Accelerator Operation (RMO).	WO
2:1	Reserved	
0	Restore Accelerator Operation State (RSO).	WO

Bit **Description**

Bit 3 When set to 1, a paused screen-to-screen accelerator operation is resumed.

When set to 0, no action is taken.

Bit 0 When set to 1, the state in the accelerator's queue is transferred to the internal registers of the accelerator.

When set to 0, no action is taken.

It is possible to set both of the above bits to 1 in a single write access in order to transfer the queued state into the accelerator and resume (or initiate) an accelerator operation.

5.10.3 ACL Sync Enable Register

This is a non-queued register
Memory offset = 32

Bit	Description	Access
7:2	Reserved.	
0	Sync Enable.	RW

Bit	Description
Bit 0	When set to 1, indicates that a write to a full queue will be "wait-stated" until the queue becomes not full. When set to 0, indicates that a write to a full queue will be ignored. It is possible to generate an interrupt when such a write is ignored, see Section 2.11.7.

5.10.4 ACL Interrupt Mask Register

This is a non-queued register
Memory offset = 34

Bit	Description	Access
7:3	Reserved.	
2	Write Fault Interrupt Enable.	RW
1	Read Interrupt Enable.	RW
0	Write Interrupt Enable.	RW

Bit	Description
Bit 2	When set to 1, enables a Write Fault Interrupt when a write to a full queue occurs (and ACL Sync Enable Register, bit 0 is 0). This is an EVENT-triggered interrupt; i.e., the interrupt line asserts when the faulting write occurs. The interrupt is cleared by a write of 1 to the Write Fault Interrupt Status bit (ACL Interrupt Status Register, bit 2). When set to 0, this interrupt is disabled.
Bit 1	When set to 1, enables a Read Interrupt when the queue is empty and the Accelerator goes from busy to idle. This is an EVENT-triggered interrupt; i.e., the interrupt line asserts when the accelerator goes from busy to idle. The interrupt is cleared by a write of 1 to the Read Interrupt Status bit (ACL Interrupt Status Register, bit 1). When set to 0, this interrupt is disabled.
Bit 0	When set to 1, enables a Write Interrupt when the queue is not full. This is a STATE-triggered interrupt; i.e., the interrupt line is asserted while the queue is in the state of being "not-full". This interrupt is cleared by disabling it. When set to 0, this interrupt is disabled.

5.10.5 ACL Interrupt Status Register

This is a non-queued register
Memory offset = 35

Bit	Description	Access
7:3	Reserved.	
2	Write Fault Interrupt Status.	RW
1	Read Interrupt Status.	RW
0	Write Interrupt Status.	RO

Bit	Description
Bit 2	A value of 1 indicates that the current interrupt condition was caused by a Write Fault When set to 1, clears the Write Fault Interrupt condition. When set to 0, the value of this bit is unaffected.
Bit 1	A value of 1 indicates that the current interrupt condition was caused by a Read Interrupt. When set to 1, clears the Read Interrupt condition. When set to 0, the value of this bit is unaffected.
Bit 0	A value of 1 indicates that the current interrupt condition was caused by a Write Interrupt. To clear the Write Interrupt, disable by setting bit 0 of the ACL Interrupt Mask Register to 0 (See Section 5.10.4)

5.10.6 ACL Accelerator Status Register

This is a non-queued register
Memory offset = 36

Bit	Description	Access
7:4	Reserved.	
3	Screen-to-Screen Status (SSO).	RO
2	XY Status (XYST).	RW
1	Read Status (RDST).	RO
0	Write Status (WRST).	RO

Bit	Description
Bit 3	A value of 1 indicates that the current Accelerator operation is a screen-to-screen operation. This bit is only valid when bit 2 is 1. It is used by State-Restore software to determine if a write to the RMO bit (ACL Operation State Register, bit 3) is necessary.
Bit 2	A value of 1 indicates that the Accelerator is processing an X/Y block. An "X/Y Block" means that the accelerator's internal XPOS, YPOS have not yet reached the terminal XCNT, YCNT for a given operation. Note that this bit must be restored when the state is restored for a suspended operation.
Bit 1	A value of 1 indicates that the Accelerator is busy (i.e., may be modifying display memory) or the queue is not empty. A value of 0 indicates that the Accelerator is idle and the queue is empty, or the Accelerator is suspended. In other words, when this bit is 0, the host is guaranteed to read correct results from the display memory and from the accelerator's internal registers.
Bits 0	A value of 1 indicates that the accelerator's queue is full, and cannot accept any more host writes. A value of 0 indicates that the accelerator's queue is not full and hence it is okay to write to a queued register or to an accelerated MMU aperture.

QUEUED REGISTERS

Queued registers are found at memory offsets in the range 80 to FF. These registers are used to set up parameters for Accelerator operations.

5.10.7 ACL Pattern Address Register

This is a queued register
Memory offset = 80

Bit	Description	Access
31:22	Reserved.	
21:0	Pattern Address.	RW

Bit	Description
Bits 21:0	This value is the absolute address in display memory for the Pattern Map. It should be programmed to point to the first byte to be processed by a given accelerated graphics operation.

5.10.8 ACL Source Address Register

This is a queued register
Memory offset = 84

Bit	Description	Access
31:22	Reserved.	
21:0	Source Address.	RW

Bit	Description
Bits 21:0	This value is the absolute address in display memory for the Source Map. It should be programmed to point to the first byte to be processed by a given accelerated graphics operation. If the host is providing data for the Source Map, the value in this register is not used by the accelerator.

5.10.9 ACL Pattern Y Offset Register

This is a queued register
Memory offset = 88

Bit	Description	Access
15:12	Reserved.	
11:0	Pattern Y Offset.	RW

Bit	Description
Bits 11:0	This value is the amount to be added to the accelerator's internal Pattern address pointer when going from one line to the next during Accelerator operations. The actual value programmed is one less than the desired number of bytes to be added. For example, if the Pattern Map is 8 pixels wide, a value of 7 should be programmed into this register.

5.10.10 ACL Source Y Offset Register

This is a queued register
Memory offset = 8A

Bit	Description	Access
15:12	Reserved.	
11:0	Source Y Offset.	RW

Bit	Description
Bits 11:0	This value is the amount to be added to the accelerator's internal Source address pointer when going from one line to the next during Accelerator operations. The actual value programmed is one less than the desired number of bytes to be added. For example, if the Source Map is 640 pixels wide, a value of 639 should be programmed into this register.

5.10.11 ACL Destination Y Offset Register

This is a queued register
Memory offset = 8C

Bit	Description	Access
15:12	Reserved.	
11:0	Destination Y Offset.	RW

Bit	Description
Bits 11:0	This value is the amount to be added to the accelerator's internal Destination address pointer when going from one line to the next during Accelerator operations. The actual value programmed is one less than the desired number of bytes to be added. For example, if the Destination Map is 640 pixels wide, a value of 639 should be programmed into this register.

5.10.12 ACL Virtual Bus Size Register

This is a queued register
Memory offset = 8E

Bit	Description	Access
7:2	Reserved.	
1:0	Virtual Bus Size (VBS).	RW

Bit **Description**

Bits 1:0 The Virtual Bus Size is only enforced when the host is providing Source Map data or Mix Map data to an accelerated operation. It is encoded as follows:

VBS	
00	1-byte
01	2-byte
10	4-byte
11	Reserved

The Host Interface of the ET4000/W32 waits for this many bytes and then releases the data to the accelerator. The Virtual Bus Size also controls the amount addresses are to be incremented for each host data transfer to the accelerator. The increment value also depends on the ADRO and DARO values (see Section 5.10.20, ACL Routing Control Register):

VBS	ADRO	DARO	Increment
xx	00	000	N/A (No CPU data transfer)
xx	01	000	1-byte
00	xx	001	1-byte
01	xx	001	2-bytes
10	xx	001	4-bytes
00	xx	010	8-bytes
01	xx	010	16-bytes
10	xx	010	32-bytes
11	xx	xxx	Reserved

5.10.13 ACL X/Y Direction Register

This is a queued register
Memory offset = 8F

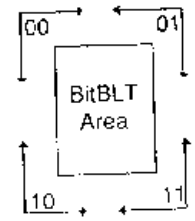
Bit	Description	Access
7:2	Reserved.	RW
1	Y Direction.	RW
0	X Direction.	

Bit **Description**

Bits 1:0 These bits indicate in which direction the accelerated operation will proceed.

When set to 0, the Accelerator operates from the lowest address to highest address (increasing direction).

When set to 1, the Accelerator operates from highest address to lowest address (decreasing direction). The figure below summarizes the effect of various programmed values:



5.10.14 ACL Pattern Wrap Register

This is a queued register
Memory offset = 90

Bit	Description	Access
7	Reserved.	
6:4	Pattern Y Wrap (PYWR).	RW
3	Reserved.	
2:0	Pattern X Wrap (PXWR).	RW

Bit	Description
Bits 6:4 Bits 2:0	The Pattern X Wrap and Pattern Y Wrap fields define an x-by-y tile size for the Pattern Map. After the Accelerator operates on the wrap-length number of bytes (horizontally) or lines (vertically), the Pattern pointer is set back wrap-length number of bytes or lines. The Source map has wrap control registers that are identical to the Pattern.

Pattern X Wrap	Horizontal Wrap Length
000	Reserved
001	Reserved
010	4 byte
011	8-byte
100	16-byte
101	32-byte
110	64-byte
111	No wrap

Pattern Y Wrap	Vertical Wrap Length
000	1-line
001	2-line
010	4-line
011	8-line
100	Reserved
101	Reserved
110	Reserved
111	No wrap

5.10.15 ACL Source Wrap Register

This is a queued register
Memory offset = 92

Bit	Description	Access
7	Reserved.	
6:4	Source Y Wrap (SYWR).	RW
3	Reserved.	
2:0	Source X Wrap (SXWR).	RW

Bit	Description
Bits 6:4 Bits 2:0	See Section 5.10.14, ACL Pattern Wrap Register for an explanation of this register.

5.10.16 ACL X Position Register

This is a queued register
Memory offset = 94

Bit	Description	Access
15:12	Reserved.	
11:0	X Position.	RW

Bit	Description
Bits 11:0	Reading this register returns the accelerator's internal X Position, indicating how far it has progressed through a given graphics operation. As the accelerator is running, this register is constantly changing; starting from the value written into this register and approaching the terminal value as programmed in the ACL X Count Register. Writing to this register will load the X Position Register in the queue, but will not affect the accelerator's internal copy of this register; thus if the host attempts to read back a value just written, the values will not match. The X and Y Position registers are used only for saving and restoring the Accelerator's current position when it is suspended in the middle of an operation. They should normally be initialized to zero at power-up, the software should ensure that they are zero when any accelerated operation is initiated.

5.10.17 ACL Y Position Register

This is a queued register
Memory offset = 96

Bit	Description	Access
15:12	Reserved.	
11:0	Y Position.	RW

Bit	Description
Bits 11:0	See Section 5.10.16, ACL X Position Register for an explanation of this register.

5.10.18 ACL X Count Register

This is a queued register
Memory offset = 98

Bit	Description	Access
15:12	Reserved.	
11:0	X Count.	RW

Bit	Description
Bits 11:0	This value specifies the number of bytes in the X dimension on which the accelerator should operate. The X Count should be programmed to one less than the desired number of bytes to be operated on.

5.10.19 ACL Y Count Register

This is a queued register
Memory offset = 9A

Bit	Description	Access
15:12	Reserved.	
11:0	Y Count.	RW

Bit	Description
Bits 11:0	This value specifies the number of lines in the Y dimension on which the accelerator should operate. The Y Count should be programmed to one less than the desired number of lines to be operated on.

5.10.20 ACL Routing Control Register

This is a queued register
Memory offset = 9C

Bit	Description	Access
7:6	Reserved.	
5:4	Routing of CPU address (ADRO).	RW
3	Reserved.	
2:0	Routing of CPU data (DARO).	RW

Bit	Description
Bits 5:4	Routing of CPU address:

ADRO

00	CPU address not used
01	CPU address is Destination address
10	Reserved
11	Reserved

"CPU address not used" means only the first write to an accelerated MMU aperture is used to determine the destination address. Then, as the accelerated operation progresses, the destination pointer is updated automatically.

Bits 2:0 Routing of CPU data:

DARO

000	CPU data not used
001	CPU data is Source data
010	CPU data is Mix Data
011	Reserved
100	CPU data is X Count
101	CPU data is Y Count
11x	Reserved

When the CPU data is X Count or Y Count, the initial write to start the accelerator operation stores the low-order 8 bits of the corresponding internal X Count or Y Count register (the high-order bits come from the X Count or Y Count in the queue as normal). Note that the Virtual Bus size must be 1 byte in this case.

5.10.22 ACL Background Raster Operation Register

This is a queued register
Memory offset = 9E

Bit	Description	Access
7:0	Background Raster Operation (BGR).	RW

Bit	Description
Bits 7:0	This is the logical operation between Source, Pattern, and Destination Maps used when CPU data routing is Mix Data, and the Mix data bit is a 0 (see Section 5.10.20, ACL Routing Control Register). See also Appendix A, ET4000/W32 (Microsoft) Raster Operations Codes and Definitions.

5.10.21 ACL Reload Control Register

This is a queued register
Memory offset = 9D

Bit	Description	Access
7:2	Reserved.	
1	Enable Reload of Pattern Address.	RW
0	Enable Reload of Source Address.	RW

Bit	Description
Bit 1	When set to 1, the accelerator's Internal Pattern Address value (resulting from the previous accelerator operation) will be the starting Pattern address for the next accelerator operation. When set to 0, the programmed ACL Pattern Address value will be used as the starting Pattern address.
Bit 0	When set to 1, the accelerator's Internal Source Address value (resulting from the previous accelerator operation) will be the starting Source address for the next accelerator operation. When set to 0, the programmed ACL Source Address value will be used as the starting Source address. Note that undefined results occur if either of these bits is set to 1 when the very first accelerator operation is initiated, since the accelerator's internal address pointers are not initialized.

5.10.24 ACL Destination Address Register

This is a queued register
Memory offset = A0

Bit	Description	Access
31:22	Reserved.	
21:0	Destination Address (DA).	RW

Bit	Description
Bits 21:0	This value is the absolute address in display memory for the Destination Map. There are two methods of loading this register, explicit and implicit. An explicit load is accomplished by simply writing to this memory address, similar to any other ACL queued register. An implicit load occurs when a write is performed through an accelerated MMU aperture. When such a write is performed, the address after MMU translation (which is an absolute address into display memory) is loaded into this register.

5.10.23 ACL Foreground Raster Operation Register

This is a queued register
Memory offset = 9F

Bit	Description	Access
7:0	Foreground Raster Operation (FGR).	RW

Bit	Description
Bits 7:0	This is the logical operation between Source, Pattern, and Destination Maps used when CPU data routing is Mix Data, and the Mix data bit is a 1, or else when the CPU is not providing Mix Map data (see ACL Routing Control Register). See also Appendix A, ET4000/W32 (Microsoft) Raster Operations Codes and Definitions.